EMI & Ionizing Radiation Effects on ICs: the Need for Combined Tests

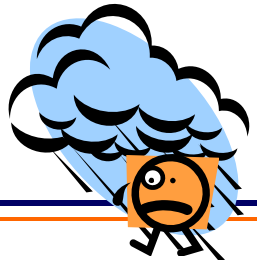
Catholic University
PUCRS

FABIAN VARGAS

ELECTRICAL ENGINEERING DEPT.
CATHOLIC UNIVERSITY – PUCRS
PORTO ALEGRE, BRAZIL

VARGAS@COMPUTER.ORG

Motivation, Main Concerns

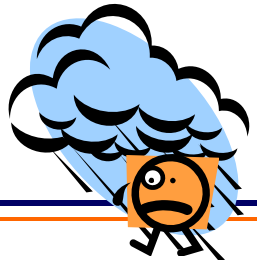


Aerospace Industry

IC & System designers are facing a continuous pressure to implement/use **new technologies**

Goal → **improve performance**, **reduce mass**, **cost** and **procurement time** for electronic equipments devoted to **critical applications** (aerospace).

Motivation, Main Concerns

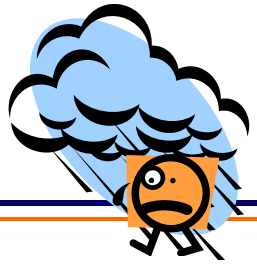


Aerospace Industry

In avionics, designs are moving from the **Federated (distributed)** to the **Centralized IMA** (**I**ntegrated **M**odular **A**vionics) Model -> multiple, mixed-critical functions (F-Control, F-Warning, Nav-System, Cabin Pressure, etc…) on a single chip!

This requires the use of **fast** (and **low power**) nano-ICs (< 100 nm) such as **processors** and **FPGAs**, which makes **EMI & radiation control** always **more challenging**.

Motivation, Main Concerns

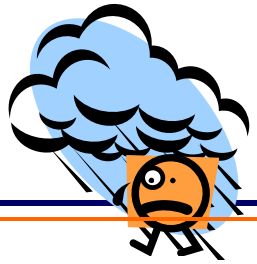


However, it is a common practice …

engineers qualify electronic systems to EMI, TID and SEU, or eventually to all of them, but often NOT taking into account the combined effects one phenomenon may take over the other.

E.g., assume that a given part of an embedded system for satellite application is certified by a set of EMI tests according to specific stds

Motivation, Main Concerns



After a given period of time operating on the field …

Who can ensure that this part will still perform properly according to the same set of EMI stds, after a given level of TID radiation has been cumulated over time on the system, if the part was certified independently for EMI and radiation?

Also, who can ensure that the system will get approved for the same set of EMI stds, if operating in a harsh environment with dense flux of high-energy particles (SEEs)?

Goal

Having said this, we ...

- analyze the impact of combined tests for EMI + radiation (TID/SEU) on the reliability of electronic components

- propose a new methodology that takes this combination into account in order to qualify state-of-the-art components

Outline

1. Understanding the effects of EMI and ionizing radiation (TID, SEE) on embedded electronics

2. Review of existing mitigation techniques

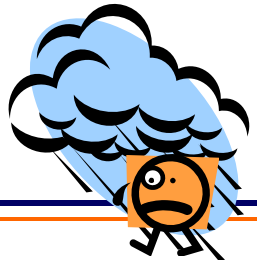
3. Combined Test Planning

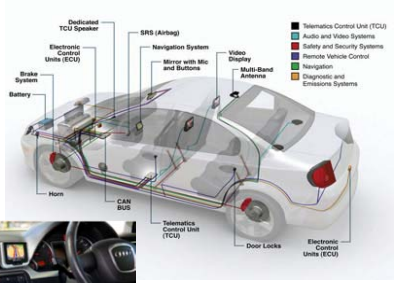
4. Configurable Platform for combined test

5. Experiments dealing to demonstrate the importance of combining these two test types for a safe system operation during whole lifetime

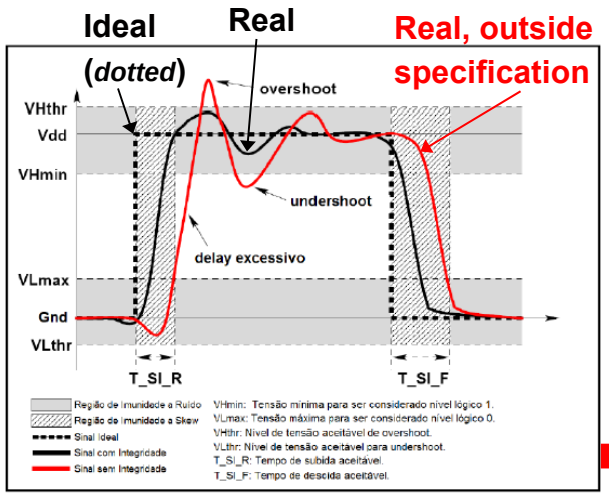
Understanding the effects of EMI on electronics

Understanding the Effects of EMI on Electronics





The **increasing hostility of the electromagnetic environment** caused by the widespread adoption of electronics, (mainly **wireless technologies**), represents a huge challenge for the reliability of RT embedded systems.



Electromagnetic Interference (EMI)

⬇

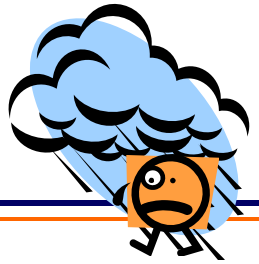
Power Supply Disturbances (PSD)

⬇

Transient Faults

➡ **Signals outside noise margins can be erroneously interpreted and stored by memory elements at the end of critical paths**

Understanding the Effects of EMI on Electronics

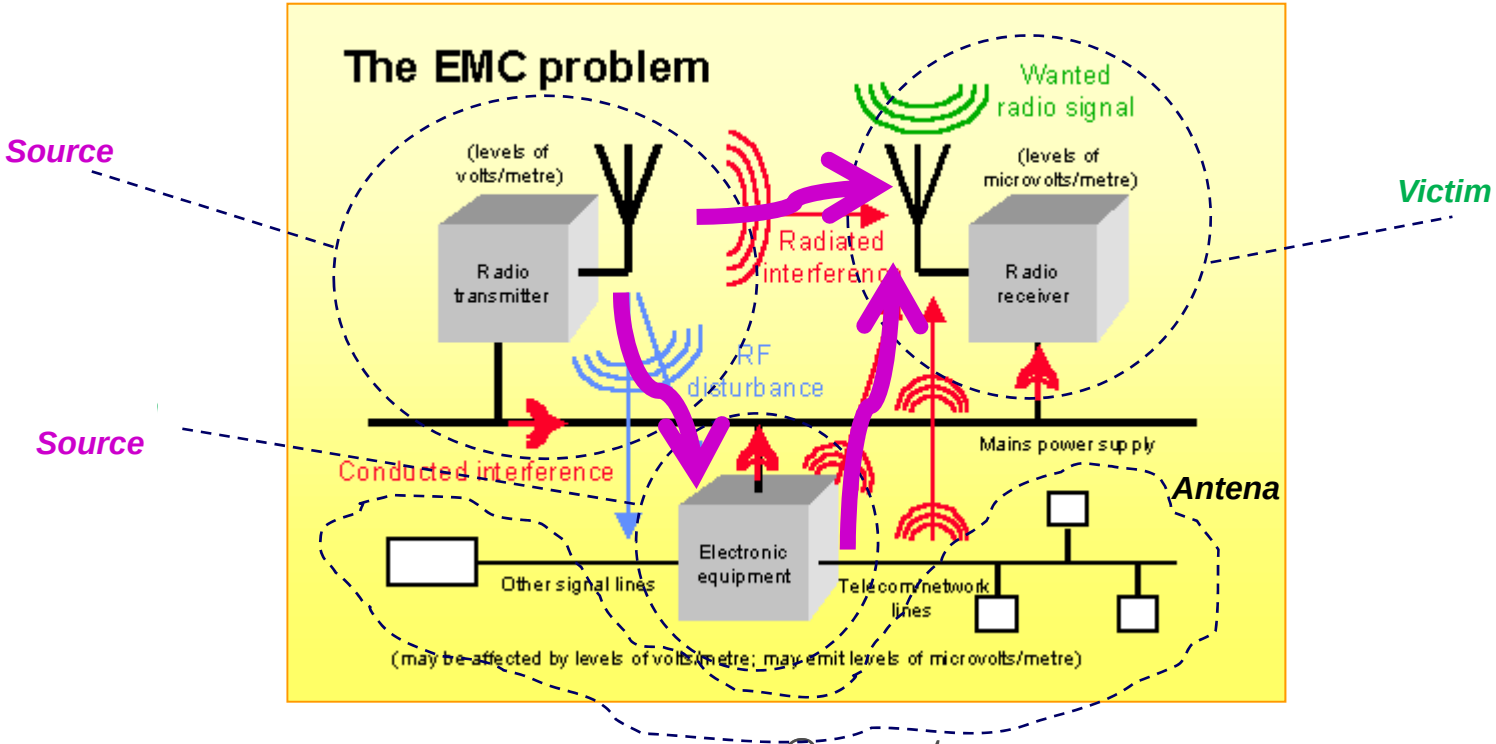


The diagram below illustrates

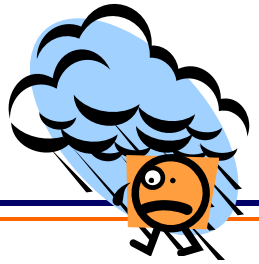
how radio transmitters can interfere with electronic systems

and

how electronic systems can interfere with radio reception



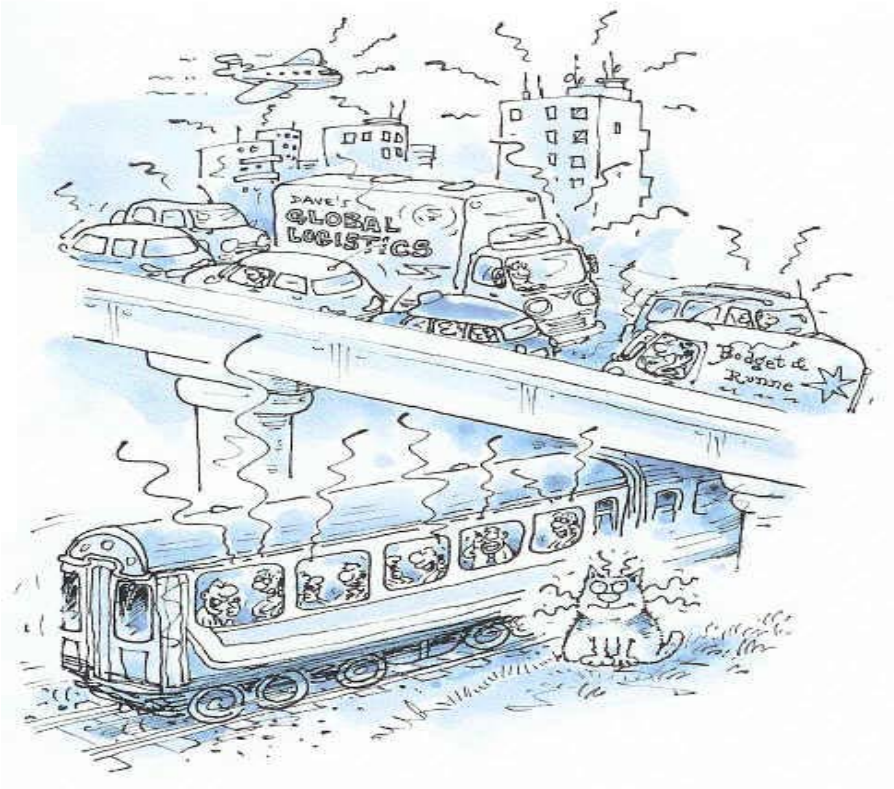
Understanding the Effects of EMI on Electronics



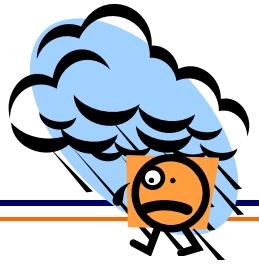
For interference to occur, we need several coincidences:

- there must exist a source of interference;
- there must exist a victim of that interference;
- there must exist a coupling path between them;
- the source must be emitting on a frequency at which the victim is susceptible;
- the source must be emitting at a time when the victim is operating;
- the interference must be at a significant level.

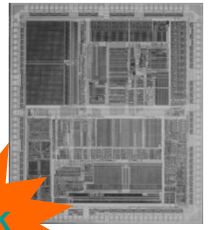
But in some occasions, when it happens …



Understanding the Effects of EMI on Electronics

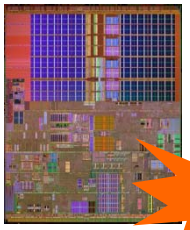


M68000 (1978),
20MHz, 5um, 3.3-5V



~100K

iPentium4 (2006),
4GHz, 65nm, 1.5V

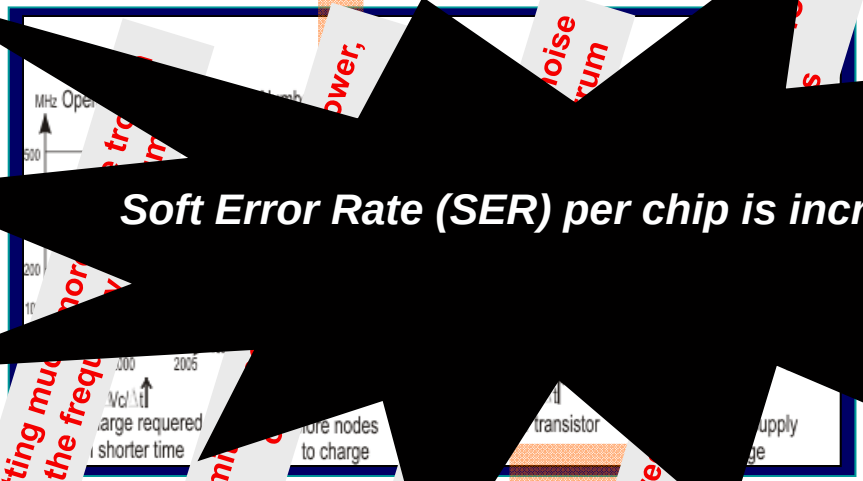


~100M

Proc? (2016/2017),
?GHz, 16nm, 0.5-1V

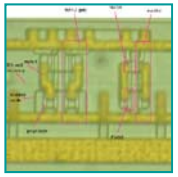
Proc?

~400M



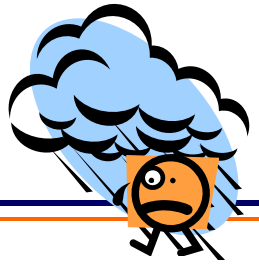
Emitting mu
the freq
Emi
ower,
oise
rum
s susceptibility,
A first hope to re

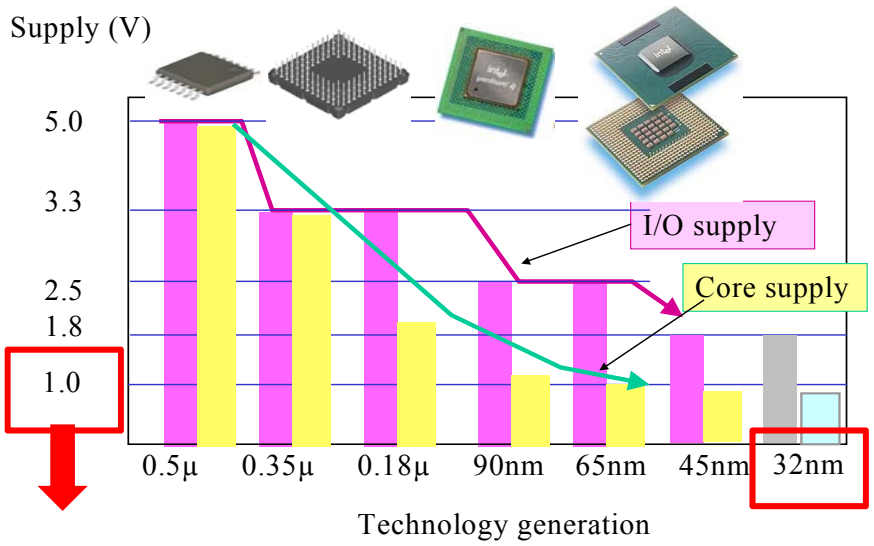
Soft Error Rate (SER) per chip is increasing



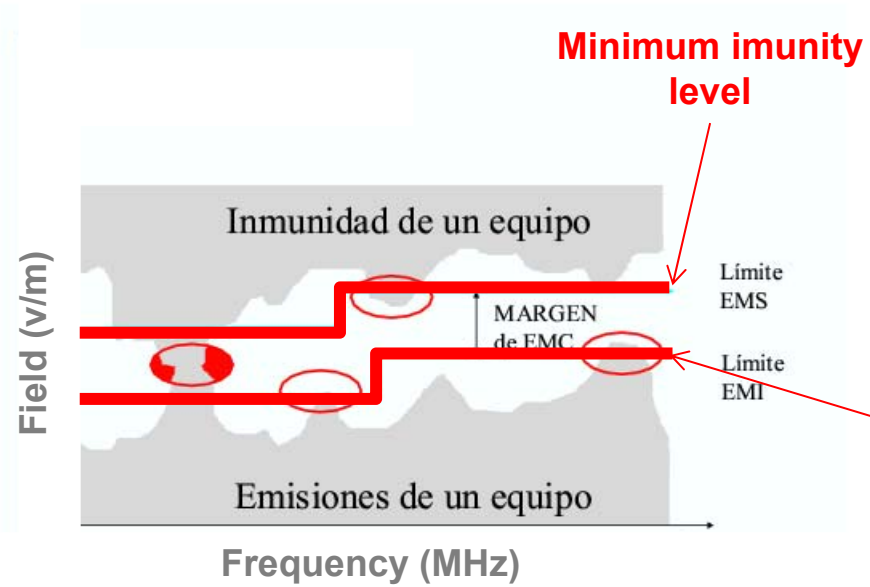
Technology tr s impact on ICs

Understanding the Effects of EMI on Electronics

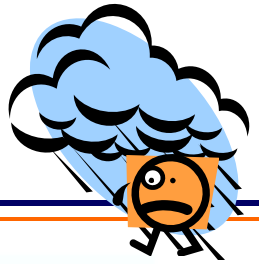




Continuous reduction of voltage supply reduces noise margins and thus, increases susceptibility



Understanding the Effects of EMI on Electronics



Muy buena antena

Antena eficiente

$\lambda = C / f$

Frecuencia de la señal	Longitud de onda	$\frac{\lambda}{4}$	$\frac{\lambda}{20}$	
50 Hz	5.000 km	1000 km	200 km	redes de distribución eléctrica, telefonía
3 kHz	100 km	25 km	5 km	
30 kHz	10 km	2,5 km	500m	instalaciones de control redes informáticas
300 kHz	1 km	250 m	50m	
3 MHz	100 m	25 m	5m	
30 MHz	10 m	2,5 m	50 cm	cables externos equipos
300 MHz	1 m	25 cm	5 cm	
3 GHz	10 cm	2,5 cm	50 mm	cables internos circuitos impresos
30 GHz	1 cm	25 mm	5 mm	
300 GHz	10 mm	2,5 mm	0,5 mm	componentes

IC input pins

EMC International Standards

www.iec.ch

System Level

IEC 61.000-4-17: Electromagnetic compatibility (EMC) – Part 4-17: Testing and measurement techniques – **Ripple on d.c. input power port immunity test**.

IEC 61.000-4-29: Electromagnetic compatibility (EMC) – Part 4-29: Testing and measurement techniques – **Voltage dips, short interruptions and voltage variations on d.c. input power port immunity tests**".

IC Level

IEC 62.132: **Measurements of Electromagnetic Immunity, 150 kHz – 1 GHz**:

Part 1: General conditions and definitions

Part 2: (G-) TEM Cell Method — Radiated Method

Part 3: Bulk Current Injection (BCI) Method

Part 4: Direct RF Power Injection Method — Conducted Methods

Part 5: Workbench Faraday Cage Method

IEC International Standards

www.iec.ch

IEC 61.000-4-17: Electromagnetic compatibility (EMC) – Part 4-17: Testing and measurement techniques – **Ripple on d.c. input power port immunity test**.

Test Levels and Waveform:

- The **preferred range of the test levels**, applicable to the d.c. power supply port of the product, are:

Level	Percentage of the nominal d.c. voltage
1	2
2	5
3	10
4	15
x	x

NOTE – "x" is an open level. This level can be given in the product specification. For the duration of the test, see 8.2.

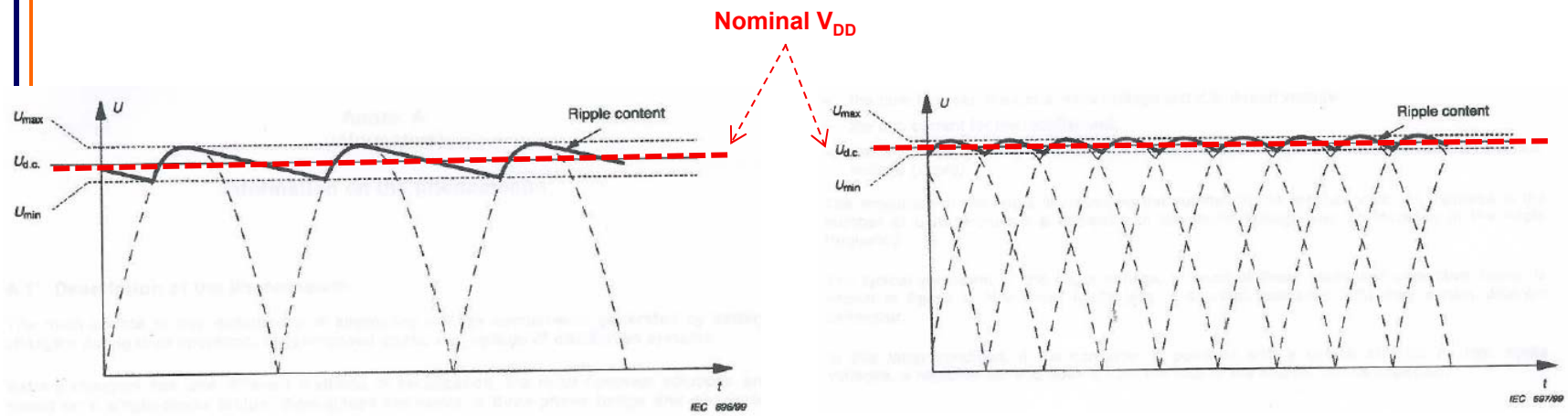
- The waveform of the ripple voltage, at the output of the test generator, has a **sinusoid-linear character**.

IEC International Standards

www.iec.ch

IEC 61.000-4-17: Electromagnetic compatibility (EMC) – Part 4-17: Testing and measurement techniques – **Ripple on d.c. input power port immunity test**.

Information on the waveform:



Single-phase rectifier

Three-phase rectifier

Examples of ripple voltage waveforms

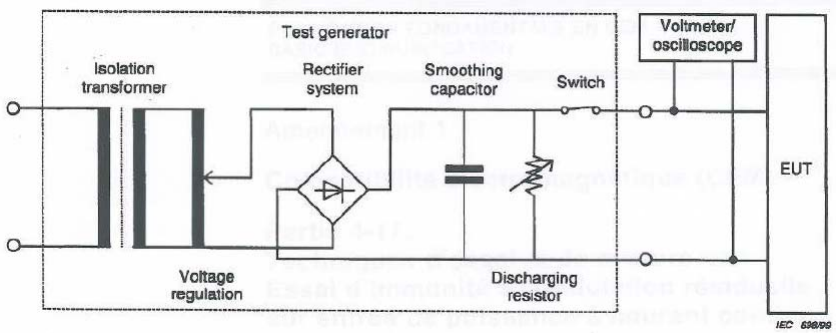
IEC International Standards

www.iec.ch

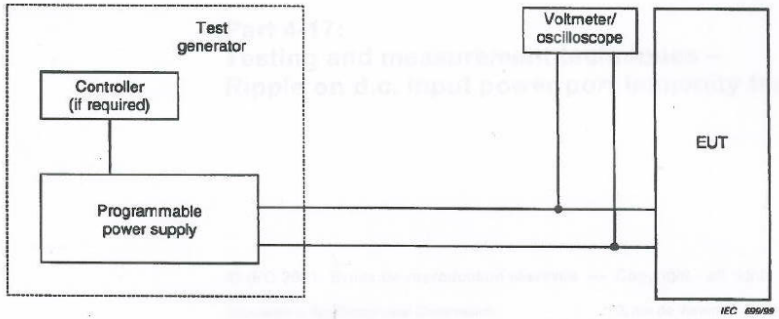
IEC 61.000-4-17: Electromagnetic compatibility (EMC) – Part 4-17: Testing and measurement techniques – **Ripple on d.c. input power port immunity test**.

Information on the generator:

The generation of the ripple voltage can be achieved in different ways: with an a.c. voltage regulator (i.e., a rectifier system with smoothing capacitor and a discharging resistor).



Example of generator based on **rectifier system**



Example of generator based on **programmable instrumentation**

IEC International Standards

www.iec.ch

IEC 61.000-4-29: Electromagnetic compatibility (EMC) – Part 4-29: Testing and measurement techniques – **Voltage dips, short interruptions and voltage variations on d.c. input power port immunity tests**.

Test Levels:

Test	Test level % U_T	Duration s
Voltage dips	40 and 70 or x	0,01 0,03 0,1 0,3 1 x

Preferred test levels and durations for **voltage dips**

Test	Test condition	Test level % U_T	Duration s
Short interruptions	High impedance and/or Low impedance	0	0,001 0,003 0,01 0,03 0,1 0,3 1 x

Preferred test levels and durations for **short interruptions**

Test	Test level % U_T	Duration s
Voltage variations	85 and 120 or 80 and 120 or x	0,1 0,3 1 3 10 x

Preferred test levels and durations for **voltage variations**

IEC 61.000-4-17: **Ripple on d.c. input power port immunity test**.

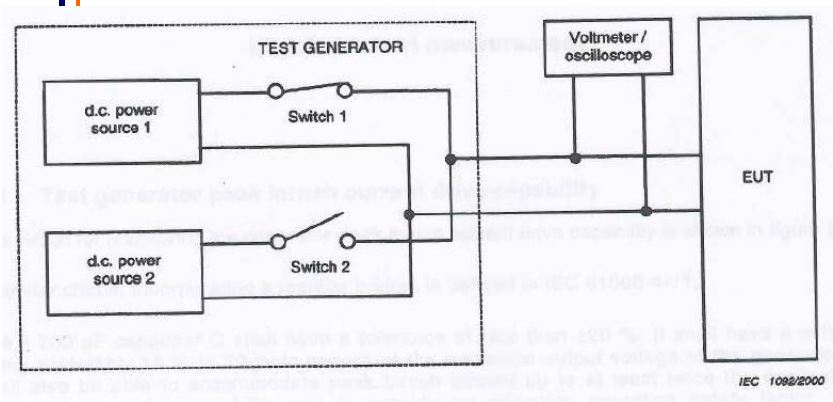
Note 1: "x" is an open value. It can be given in the product specification.

IEC International Standards

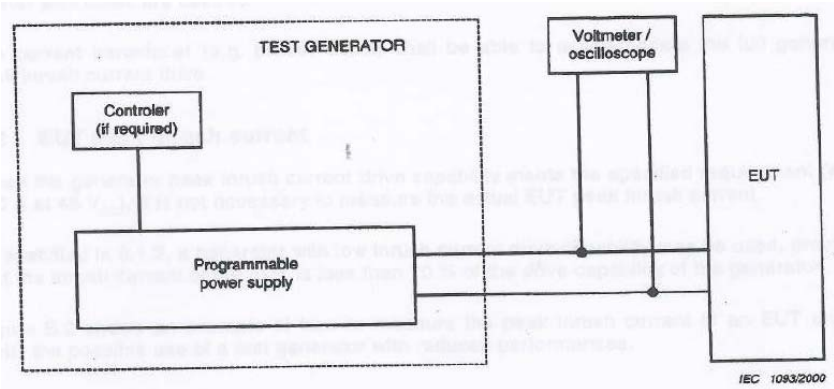
www.iec.ch

IEC 61.000-4-29: Electromagnetic compatibility (EMC) – Part 4-29: Testing and measurement techniques – **Voltage dips, short interruptions and voltage variations on d.c. input power port immunity tests**.

Information on the generator:



Example of test generator based **on two power sources with internal switching**

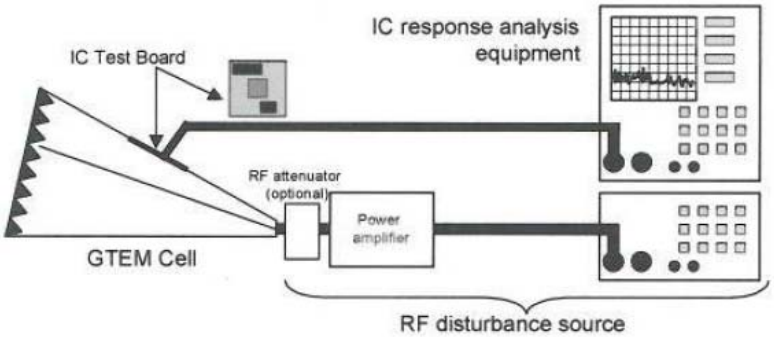


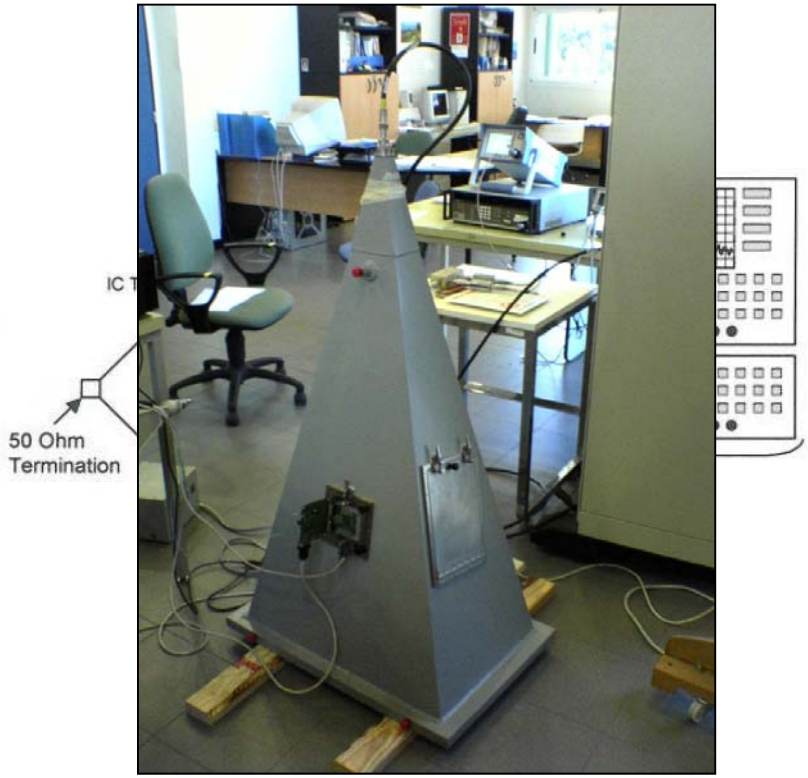
Example of test generator based on **programmable power supply**

IEC International Standards

www.iec.ch

Part 2: (G-) TEM Cell Method



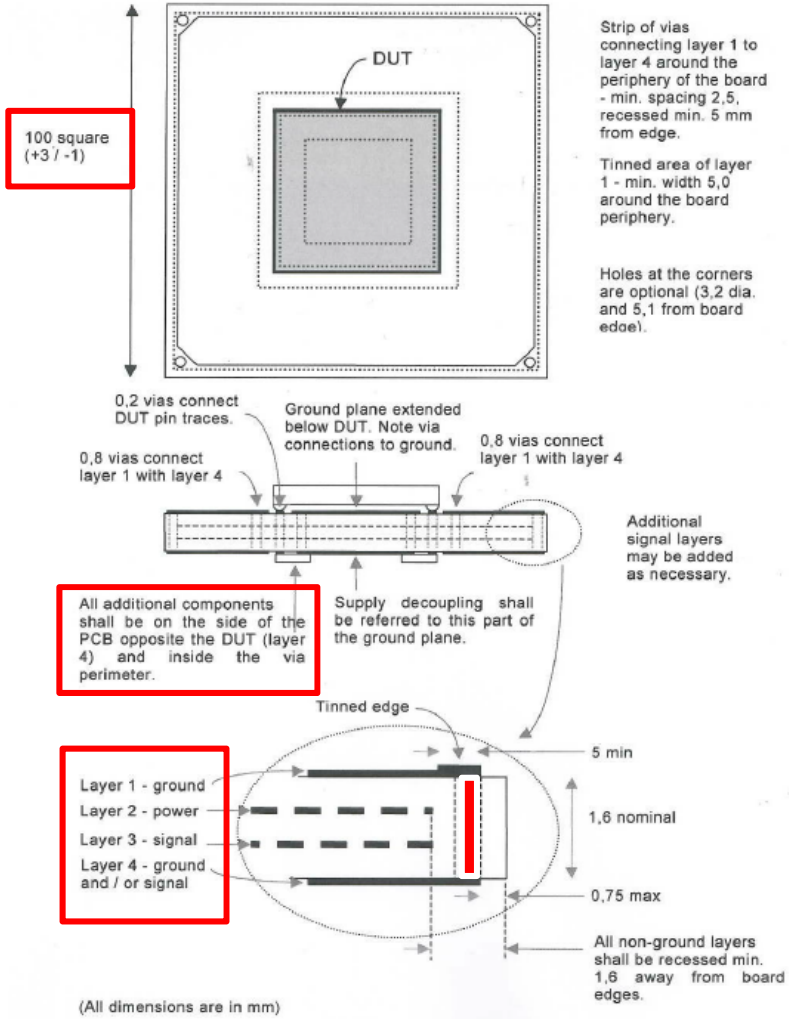


G-TEM Cell Test Setup

IEC International Standards

www.iec.ch

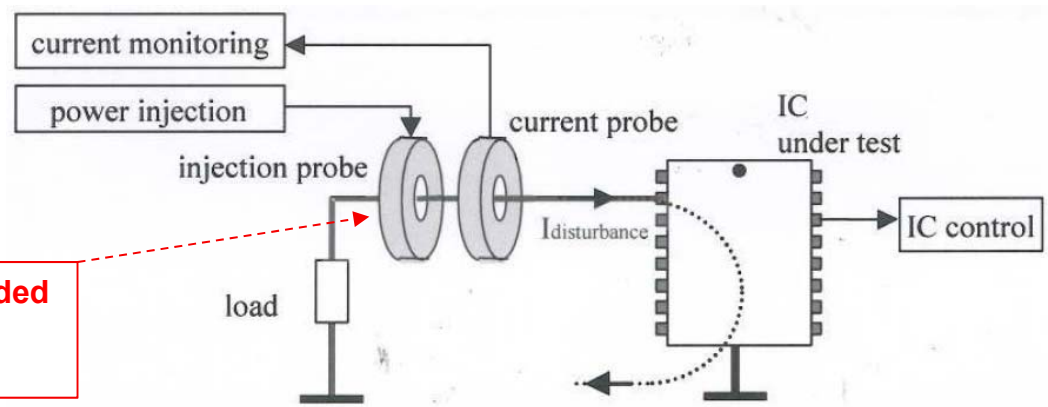
Part 2: (G-) TEM Cell Method



IC Test Printed Circuit Board for G-TEM Cell Test Method

IEC International Standards

Part 3: Bulk Current Injection (BCI) Method

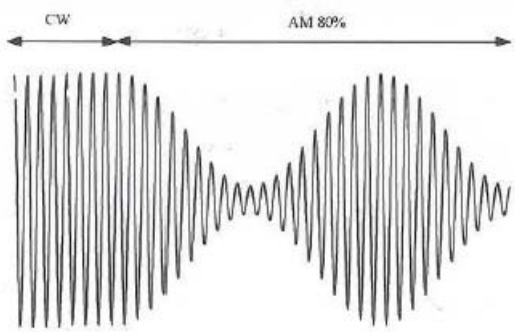


Electrically Shielded Magnetic Probes (Coils)

BCI, Hardware Test Setup

IEC International Standards

Part 3: Bulk Current Injection (BCI) Method



Constant Waveform (CW)
or
Amplitude Modulated (AM) Waveform

Test severity level	Current (CW value) No insertion loss
I	50mA
II	100mA
III	200mA
IV	300mA
V	specific value agreed between the users of this standard

Test Severity Levels

Existing Techniques to Protect Against EMI…

Increasing immunity to power supply fluctuations:

- On-chip decoupling "*power supply / core*" (near I/O ports):

(a) minimize transient currents and voltage swings (mainly on substrate, reducing Gnd bounce) and

(b) prevent external noise from entering power pins

Existing Techniques to Protect Against EMI…

Increasing immunity to power supply fluctuations:

- Perform a dedicated power distribution design by means of multiple paths to drive large amounts of current induced by fast logic switching activity ⇒ minimizes V_{DD}/Gnd bounce

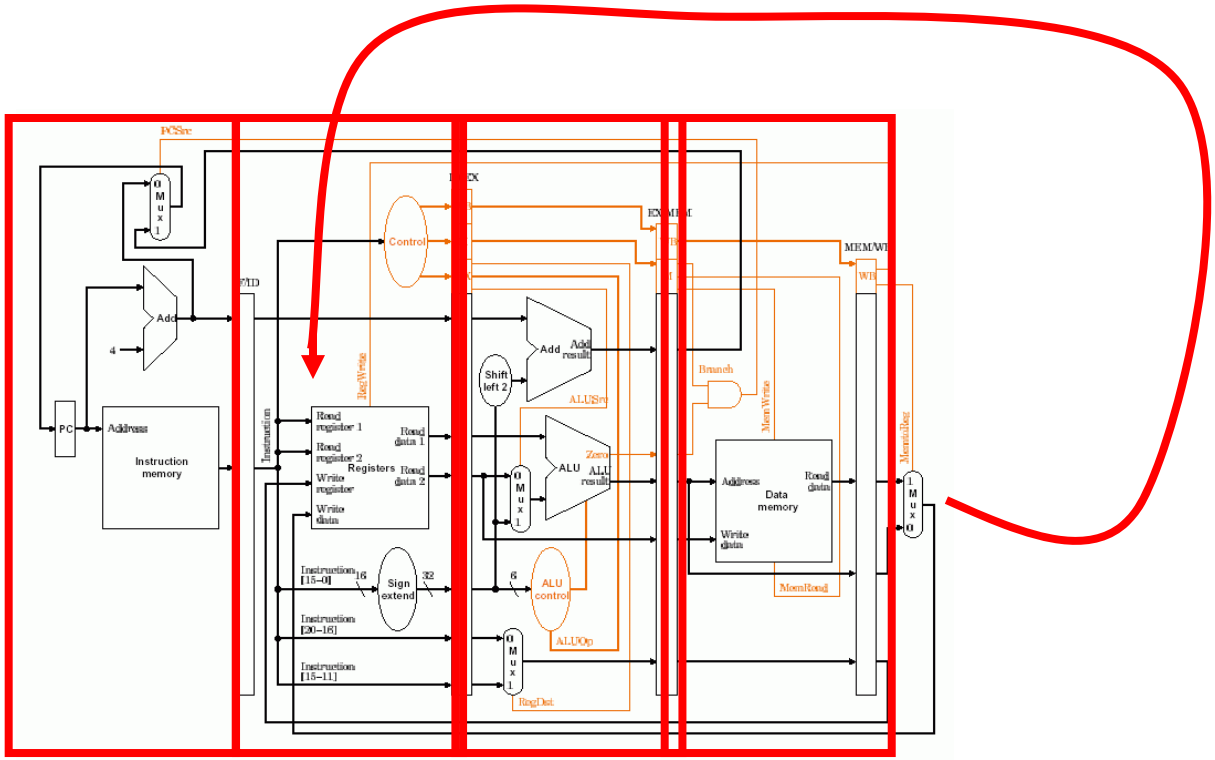
- Design circuits to work within low operating frequency rates: use of guardbands to increase noise margins

- Design of asynchronous logic by migrating existing clocked architectures or designing new ones ⇒ intrinsically delay-insensitive

DLX Processor (ASPIDA Project - Asynchronous Open-Source Ip of the Dlx Architecture)
(http://www.ics.forth.gr/carv/async/demo/)

Asynchronous Circuits and Systems Group of Institute of Computer Science – FORTH, **University of Crete**, and Microelectronics Group of **Politecnico di Torino**

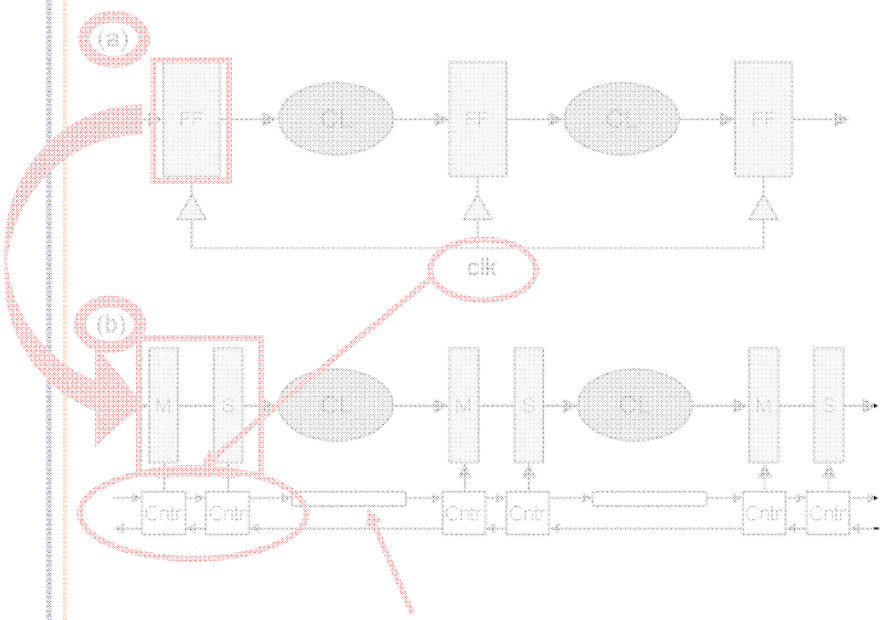
Existing Techniques to Protect Against EMI…



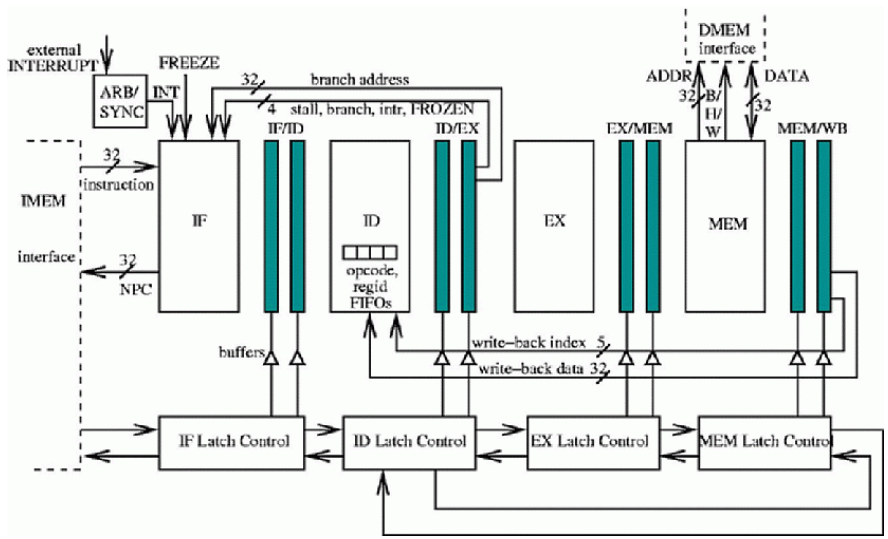
Block diagram of the synchronous DLX processor

5-Stage pipeline (Inspired on MIPS and ARM processors)

Existing Techniques to Protect Against EMI…



Desynchronization Approach:
(a) Synchronous circuit;
(b) Desynchronized version



Block diagram of the **asynchronous** ASPIDA DLX processor

Area overhead: 81%

Existing Techniques to Protect Against EMI…

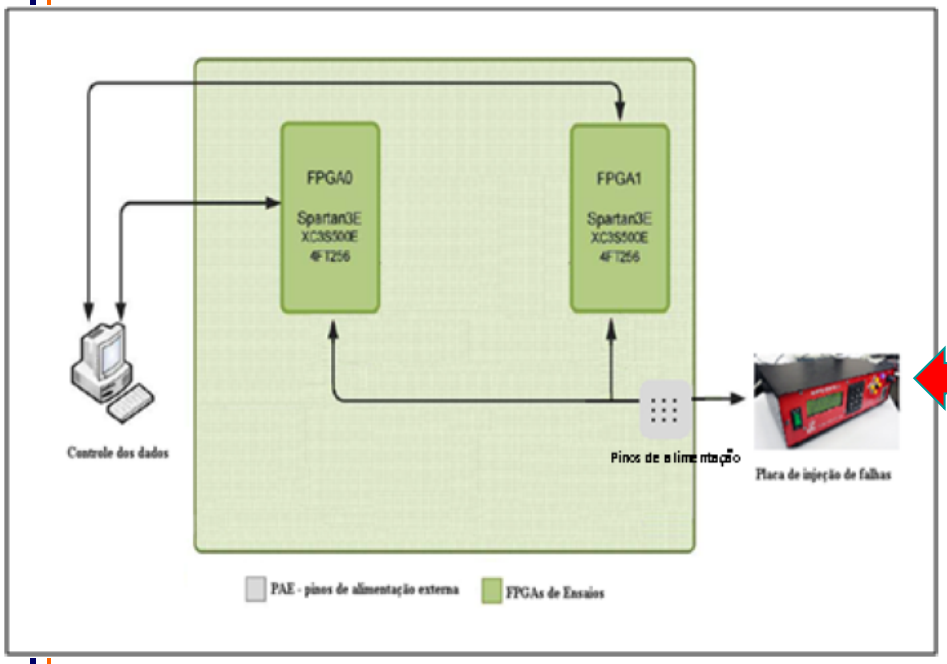
For this processor, we analyzed…

… the robustness of synchronous and asynchronous versions when exposed to EMI

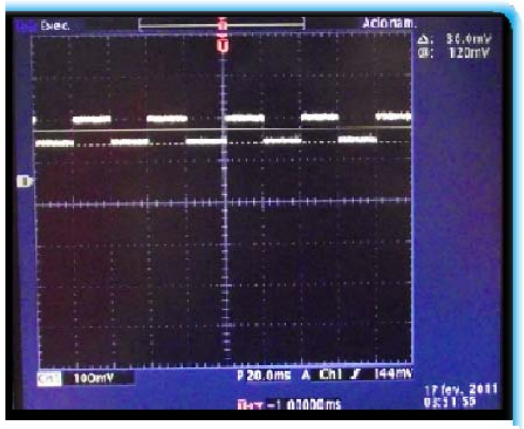
… the EM emission levels between the two design paradigms

Existing Techniques to Protect Against EMI…

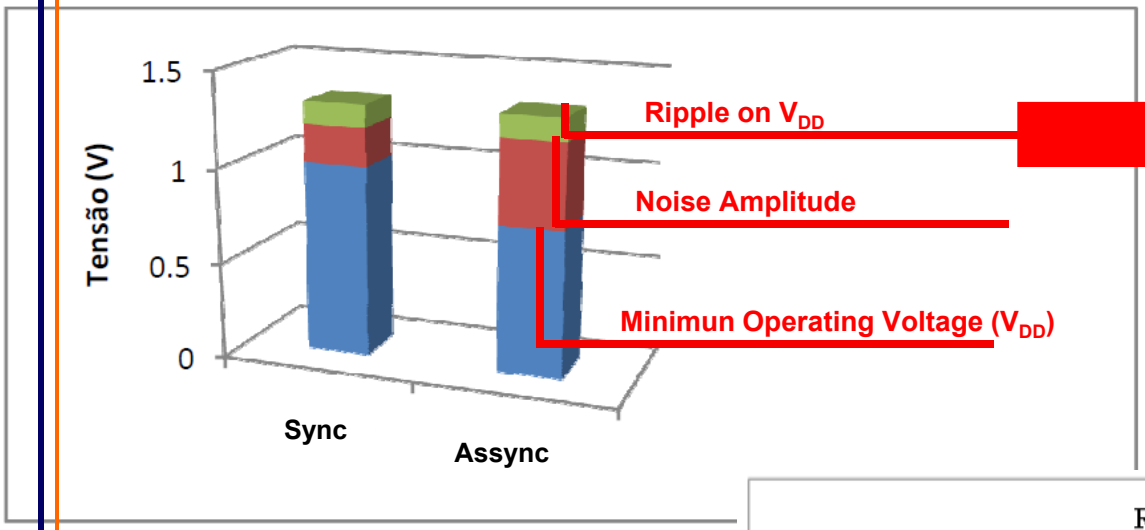
Test Conditions (Conducted EMI):

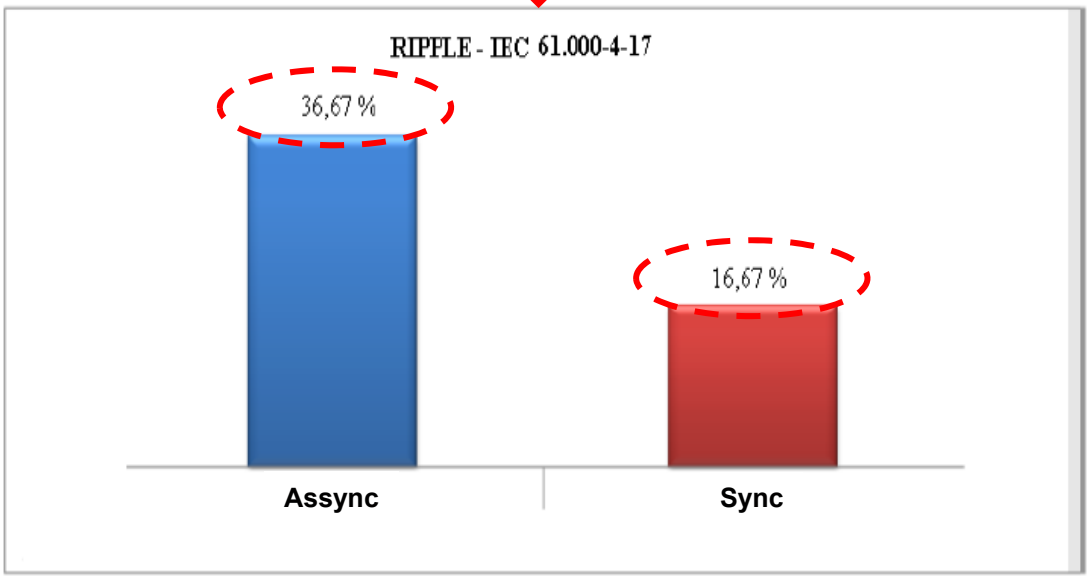


✓Based on the IEC 61.000-4-17
(Ripple on VDD bus)



Existing Techniques to Protect Against EMI…





Existing Techniques to Protect Against EMI…

Test Conditions (Radiated EMI):

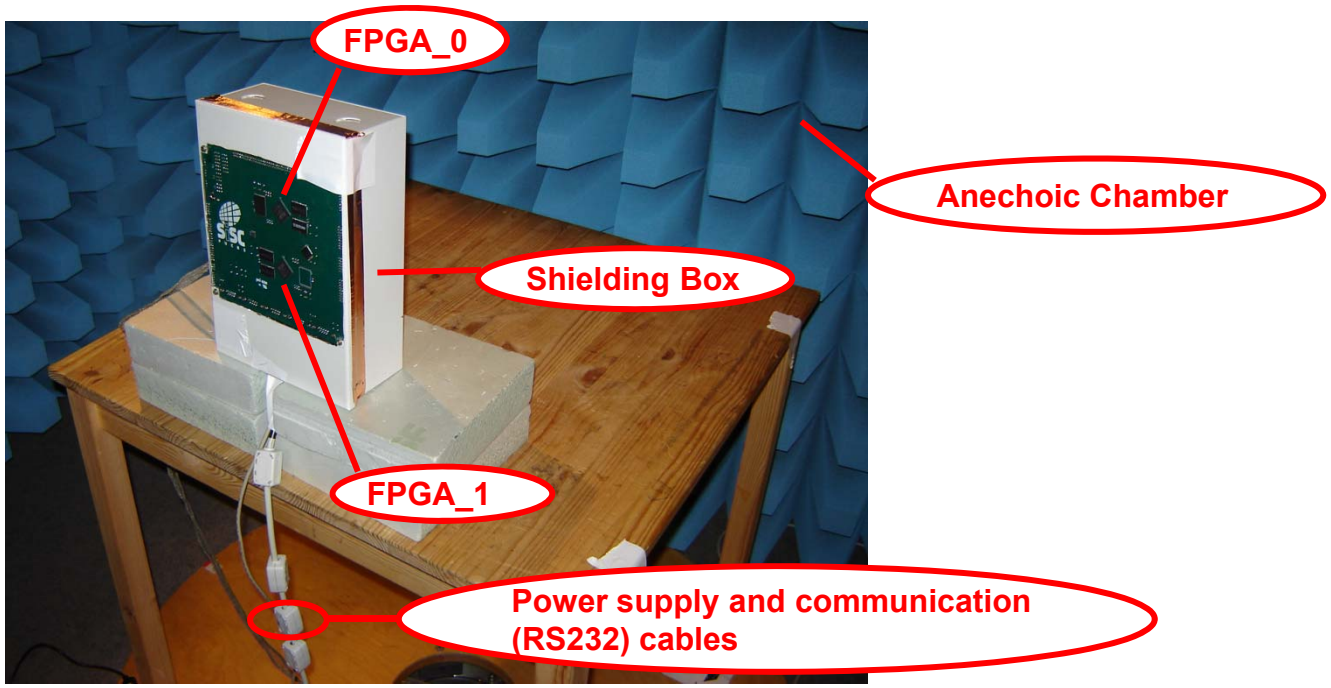
✓ **Total time of system exposition to radiated EMI: 40 hours**

✓ **For susceptibility analysis, test conditions ruled as follows:**

- EM field: 30 V/m
- Injected noise frequency range: [80KHz - 1GHz]
- Signal Modulation Format: AM 80%, with f_c at 1KHz
- Antenna Distance from the board: 1.5 meters

Existing Techniques to Protect Against EMI…

Test Environment

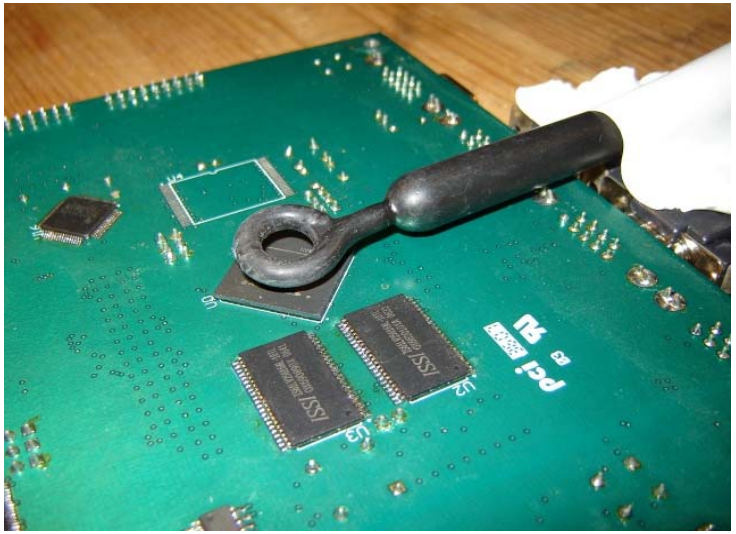


DLX Asynchronous Processor

Existing Techniques to Protect Against EMI…

Test Environment

Immunity Test



Emission Test (Near-Field Test)

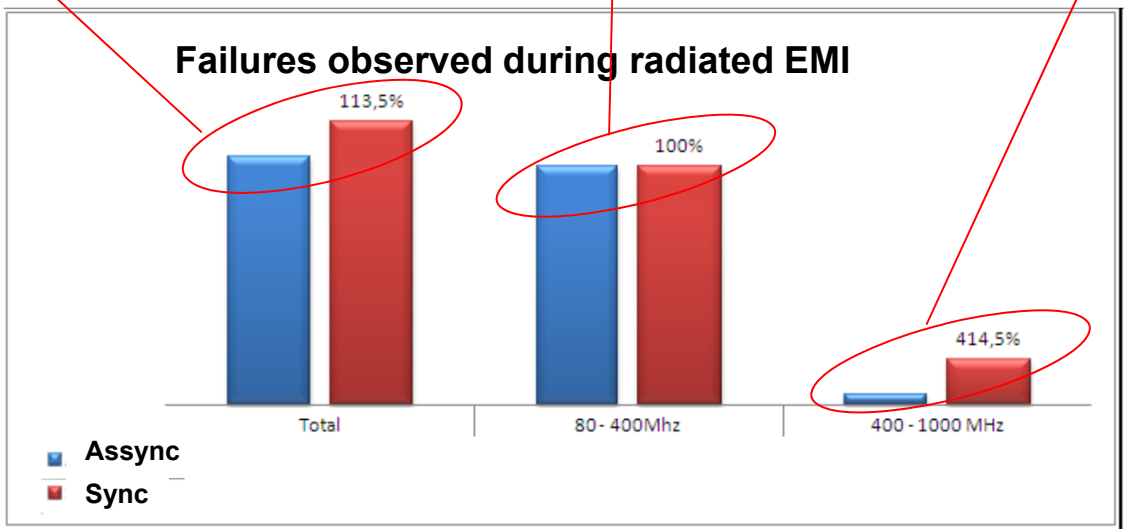
Existing Techniques to Protect Against EMI…

Synchronous x Asynchronous EM Immunity Measurements

[80-400]: Async and Sync presented similar robustness

Average: Async is 13.5% more robust than Sync version

Above 400MHz: Async is 314.5% more robust than Sync

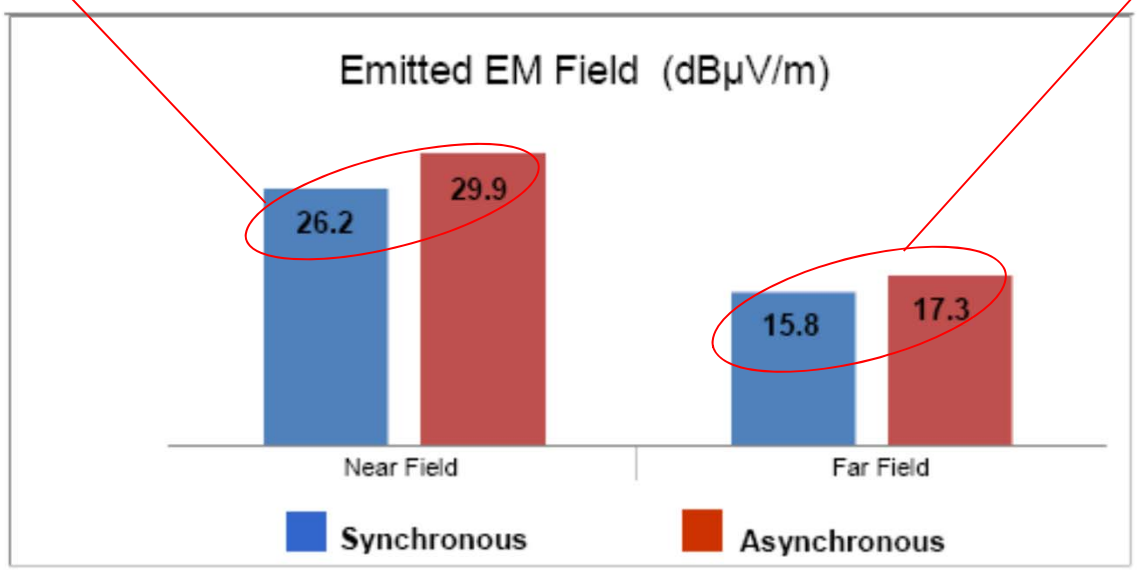


Existing Techniques to Protect Against EMI…

Synchronous x Asynchronous EM Emission Measurements

Async emits 3.7 dBuV/m above the one of the Sync version for near-field

Async emits 1.5 dBuV/m above the one of the Sync version for far-field

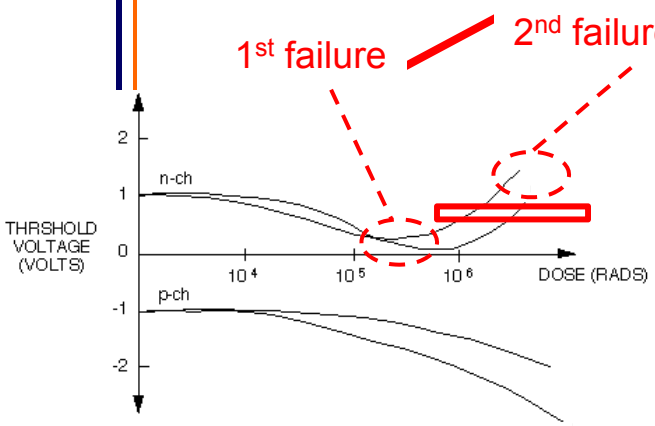


IEC 61967-2, Integrated circuits − Part 2: *Measurement of radiated emissions, TEM-cell method*;
IEC 61967-3, Integrated circuits − Part 3: *Measurement of radiated emissions, surface scan method*

Understanding the effects of radiation: TID, SEE (SEU, SET) on electronics

Understanding the Effects of Radiation (TID) on Electronics

For **critical applications** (military, aerospace or biomedical) reliability assurance to **total ionizing dose (TID) radiation** is always at a premium being a key-issue for the success of such products in the market.



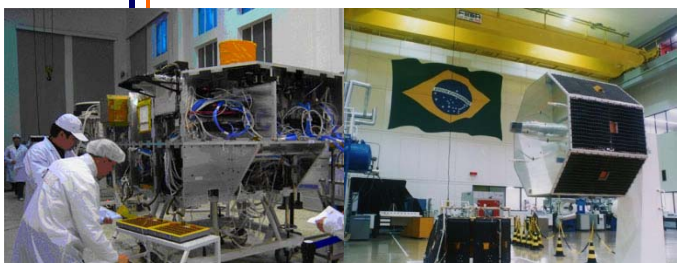
TID effects on CMOS ICs are caused primarily by **positive charge trapped in insulating layers**

⬇

For CMOS ICs, the main TID effect is the **increase of leakage currents** and **change in V_{th}** of the devices

⬇

For high doses, a **permanent functional failure** of the circuit is observed.



Understanding the Effects of Radiation (SEE) on Electronics

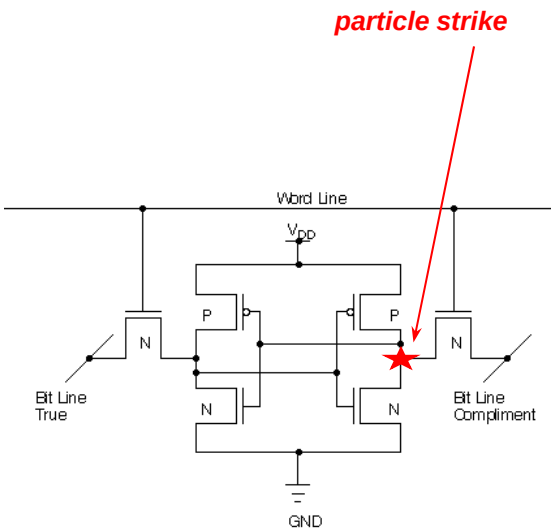
Radiation (SEU) effects on CMOS ICs are mainly caused by high-energy particles striking reverse biased drain depletion region of off-transistors

⬇

For CMOS ICs, the main SEU effect is the loss of information stored in memory elements (FFs, RAMs)

⬇

Transient functional failure of the circuit is observed



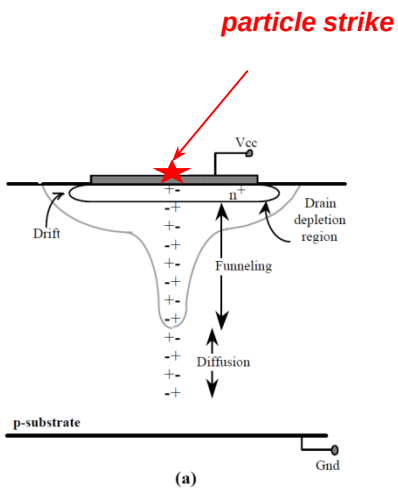
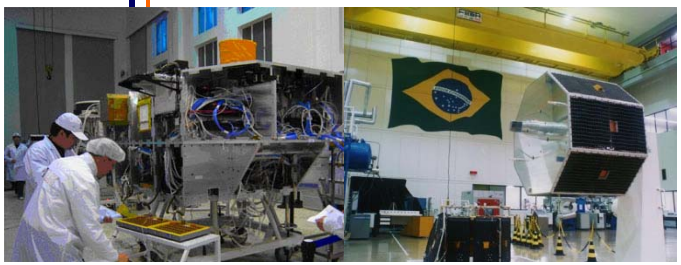


Fig. 1. Illustration of the charge collection mechanism that cause single-event upset: **(a)** particle strike and charge generation; **(b)** current pulse shape generated in the n+p junction during the collection of the charge.



Understanding the Effects of Radiation (SEE) on Electronics

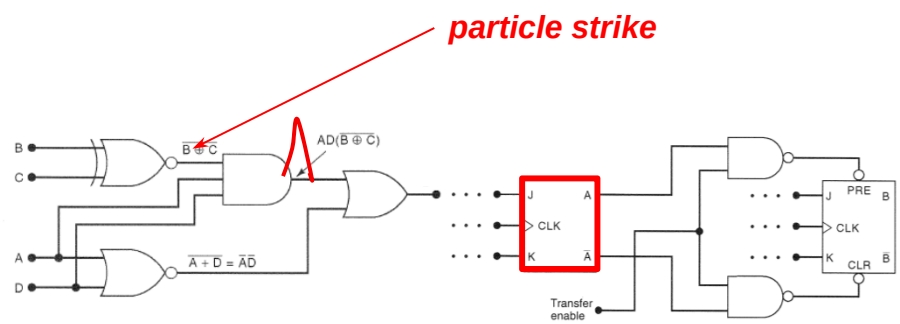
Radiation (SET) effects on CMOS ICs are mainly caused by **high-energy particles striking logic along with critical paths**

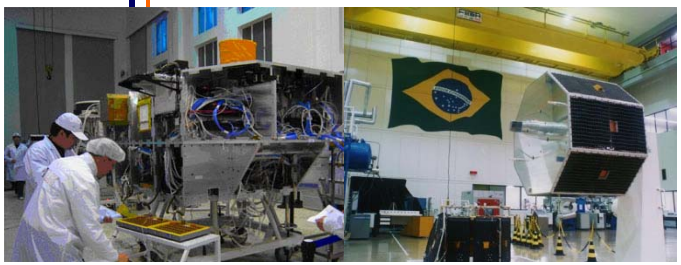
⬇

For CMOS ICs, the main SET effect is the **loss of information stored in memory elements** (FFs, RAMs)

⬇

Transient functional failure
of the circuit is observed





Existing Techniques to Protect Against Radiation

For TID:

- ***use of rad-hard fabrication process (expensive solution): SOI, bulk-epi layer, ...***

- ***use of guardbands: slow down clock frenquency, put extra timing margins***

- **use of TID-tolerant std cells library (build-up pMOS devices much larger than nMOS devices, replace NOR gates by Nand ones, etc ....)**

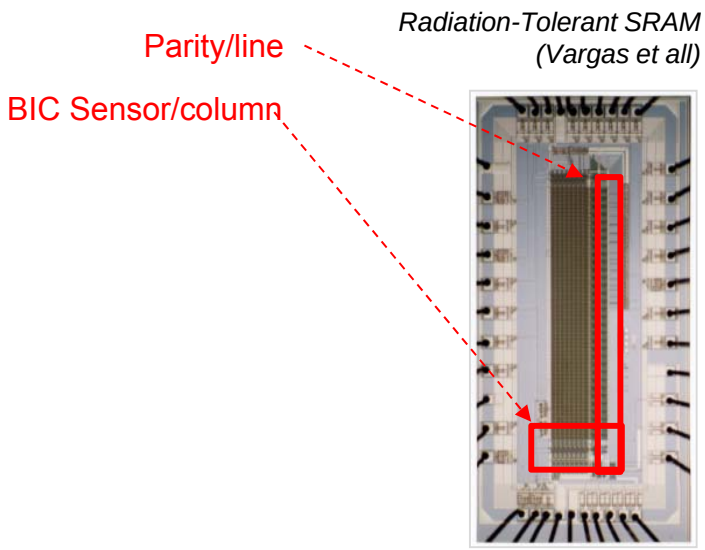
Existing Techniques to Protect Against Radiation

For SEU:

- **use of SEU-tolerant std cells library**

- ***use of EDACs (Hamming code) in memory, parity in busses, TMR (with approximate computing), Checksum, CRC, ...***

- ***use of Build-In Current Sensors (BICSs)***



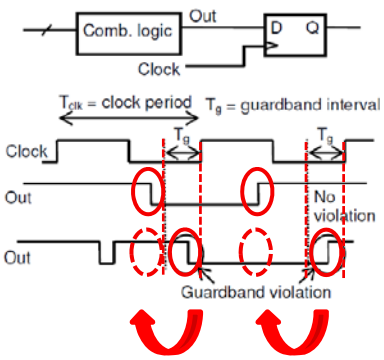
Existing Techniques to Protect Against Radiation

For SET:

- use of redundant logic (delay sensors) at the output of critical paths:

Good circuit

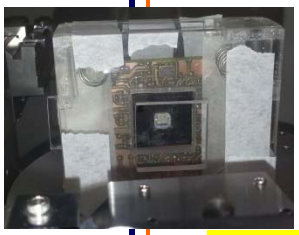
Bad circuit



Combined Test Planning

Combined Test Planning

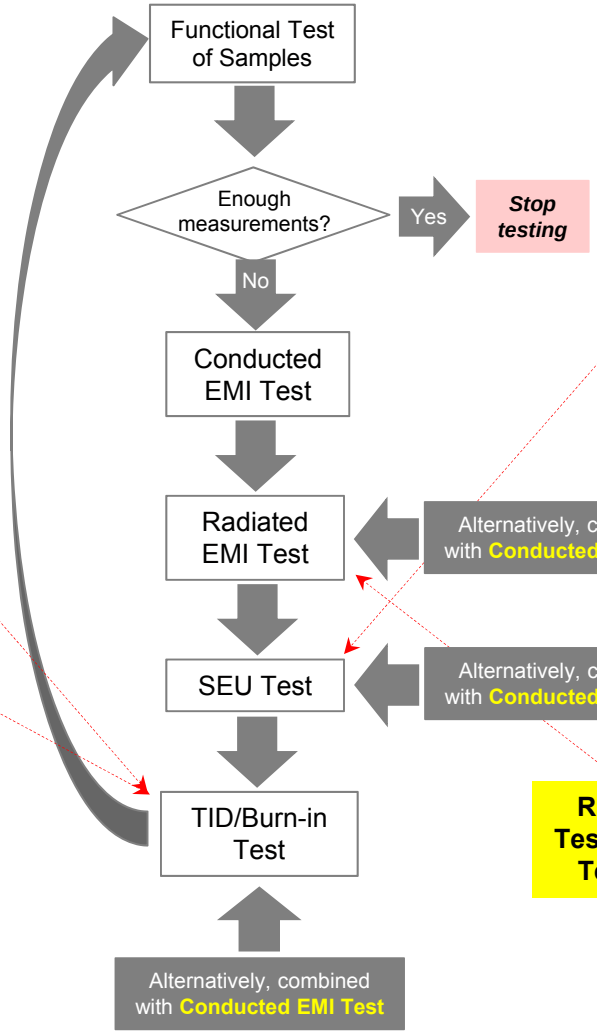
Combined tests: *EMI + Radiation*

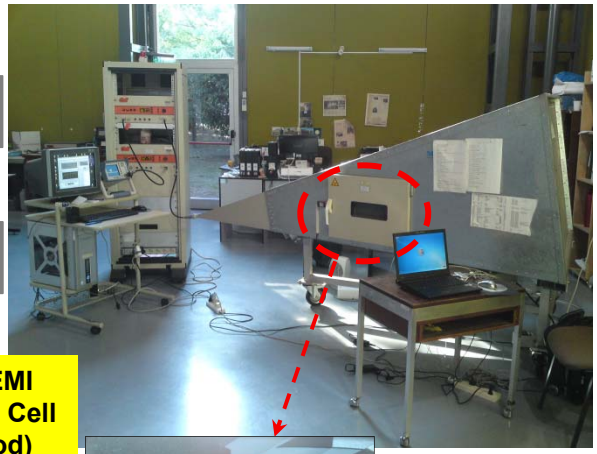


X-Ray

Co^{60} (Gamma Cell)

SEU





Radiated EMI Test (G-TEM Cell Test Method)

Configurable Platform for Combined Test of Radiation, EMI and Aging

Goal

In this context…

We have been developing a configurable platform suitable for combined tests of EMI, radiation and aging measurements of prototype embedded systems

☞ **The platform can be used to perform measurements on ICs and embedded systems having in mind EMI and radiation international stds:**

- IEC 62.132-2 (for radiated EMI noise)

- IEC 61.0004-17 and IEC 61.0004-29 (for conducted EMI noise)

and

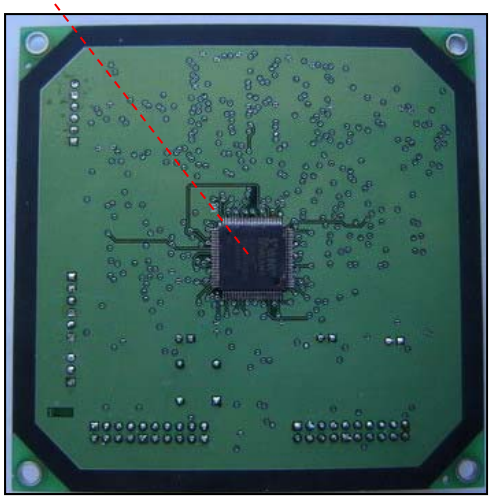
- MIL-STD-883H / 1019.4 & 1032.1 methods (for TID & SEU Test Procedures)

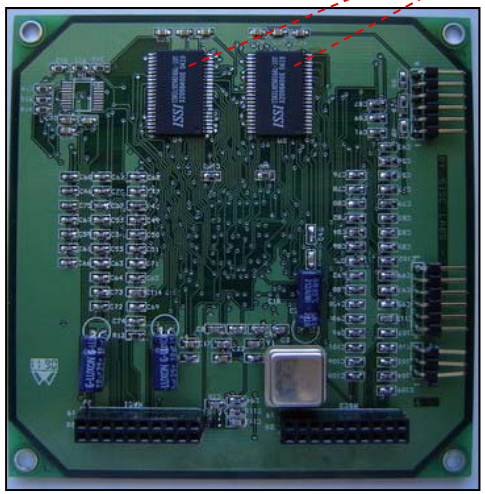
Platform (HW parts)

FPGA (System-on-Chip)

16MB SRAM (RTOS
+
user application)

System under Test





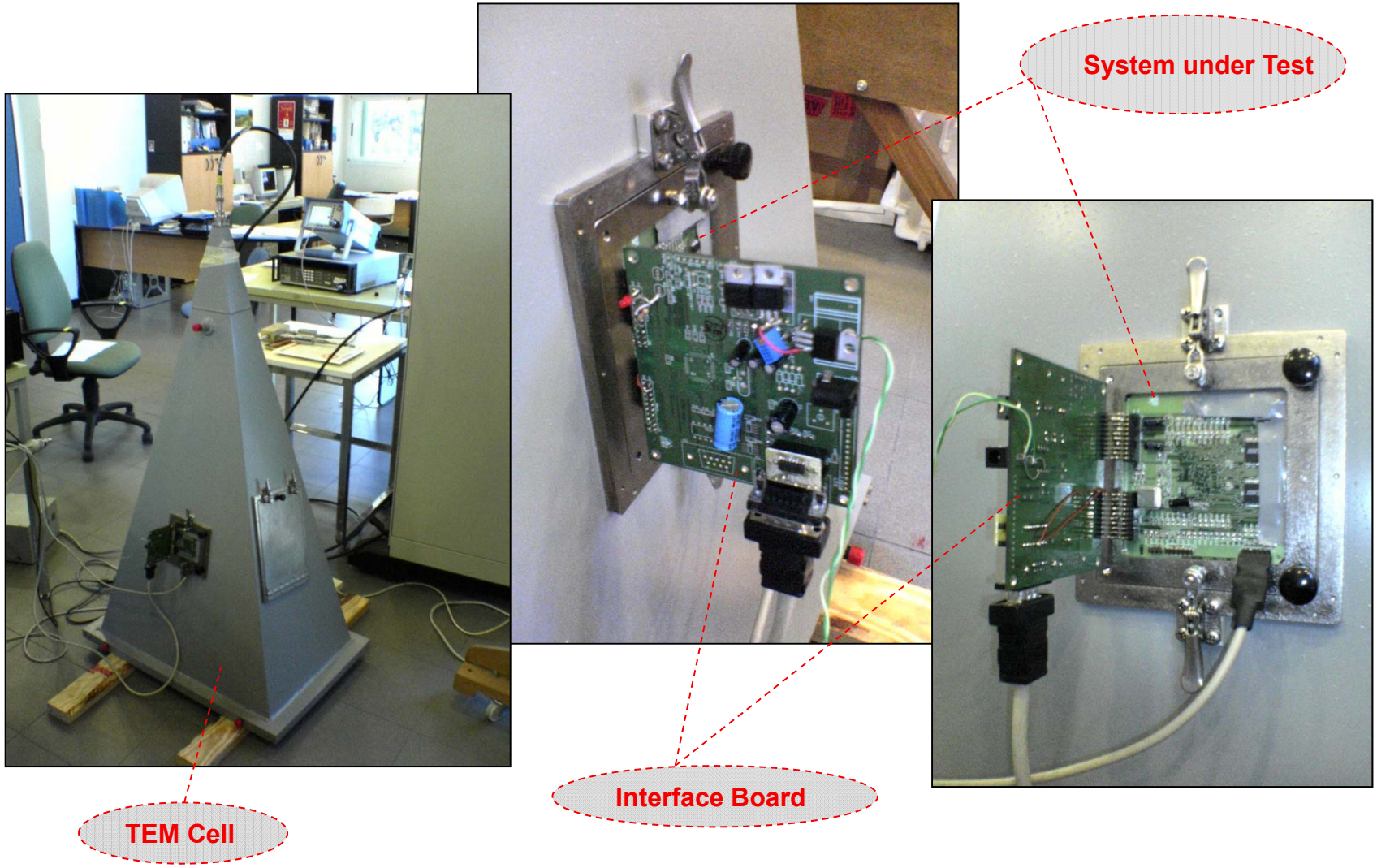
Top view

Bottom view

IEC 62.132-2 std compliant board.

Four-layers: Gnd (top) - signal - signal - Vdd (botton).

Platform (HW parts)



Platform (HW parts)

2nd

Power Supplies

Temp Sensor

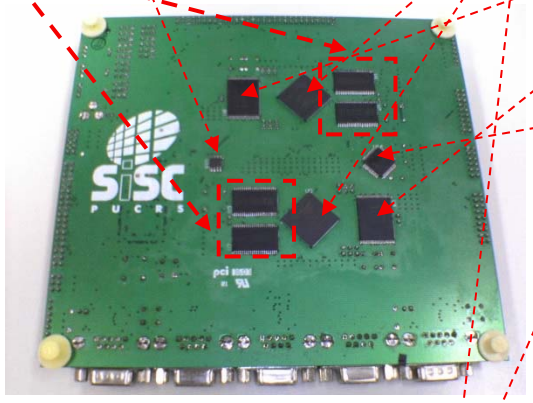
FPGA

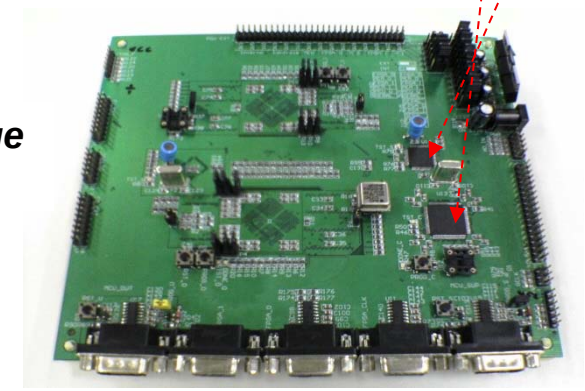
Flash

SRAM

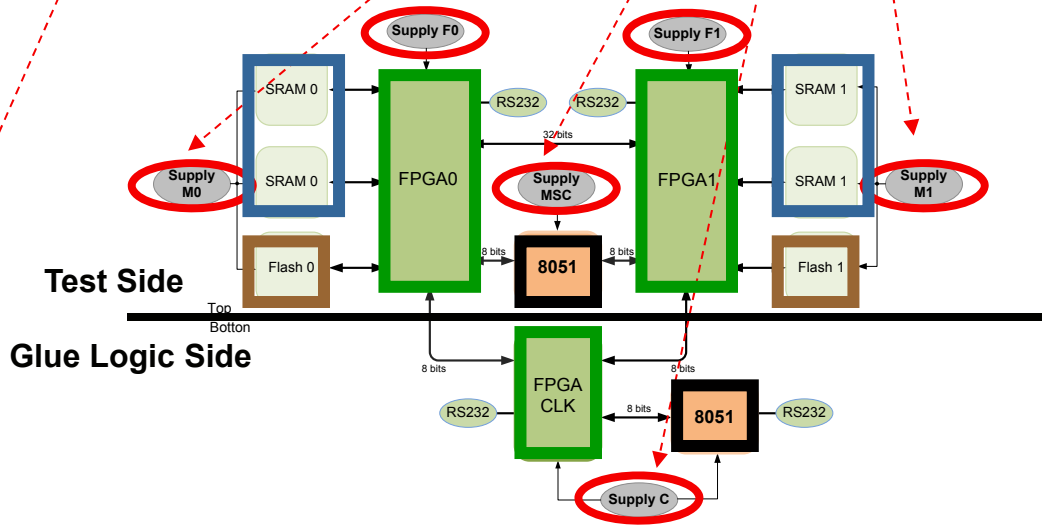
8051

Test Side





Remaining Glue Logic Side



Test Side

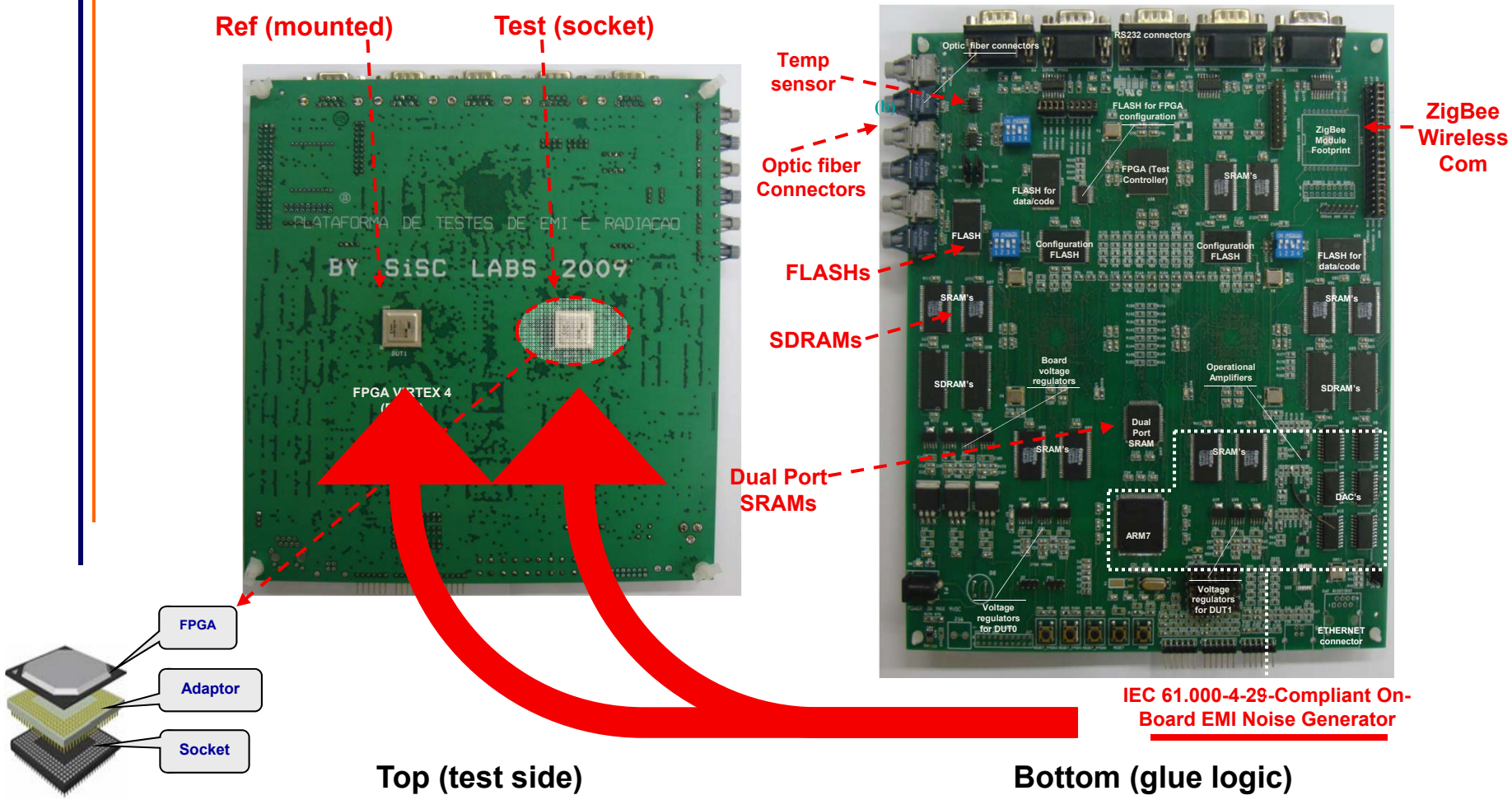
Glue Logic Side

Block Diagram

Test board designed for IEC 62.132-2 and 61.004-29 electromagnetic susceptibility analysis

3rd

Platform (HW parts)



IEC 61.000-4-29-Compliant On-Board EMI Noise Generator

Top (test side)

Bottom (glue logic)

8-layer Motherboard for Combined EMI x Radiation tests

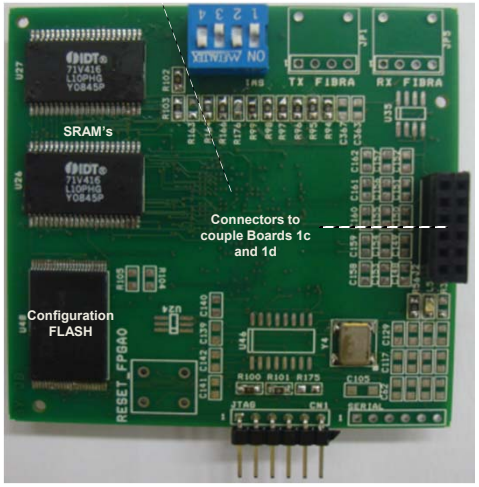
Mounting the FPGA on boards for EMI,TID, Burn-in immunity tests

Platform (HW parts)

(c)

Test FPGA
(Socket)

(d)



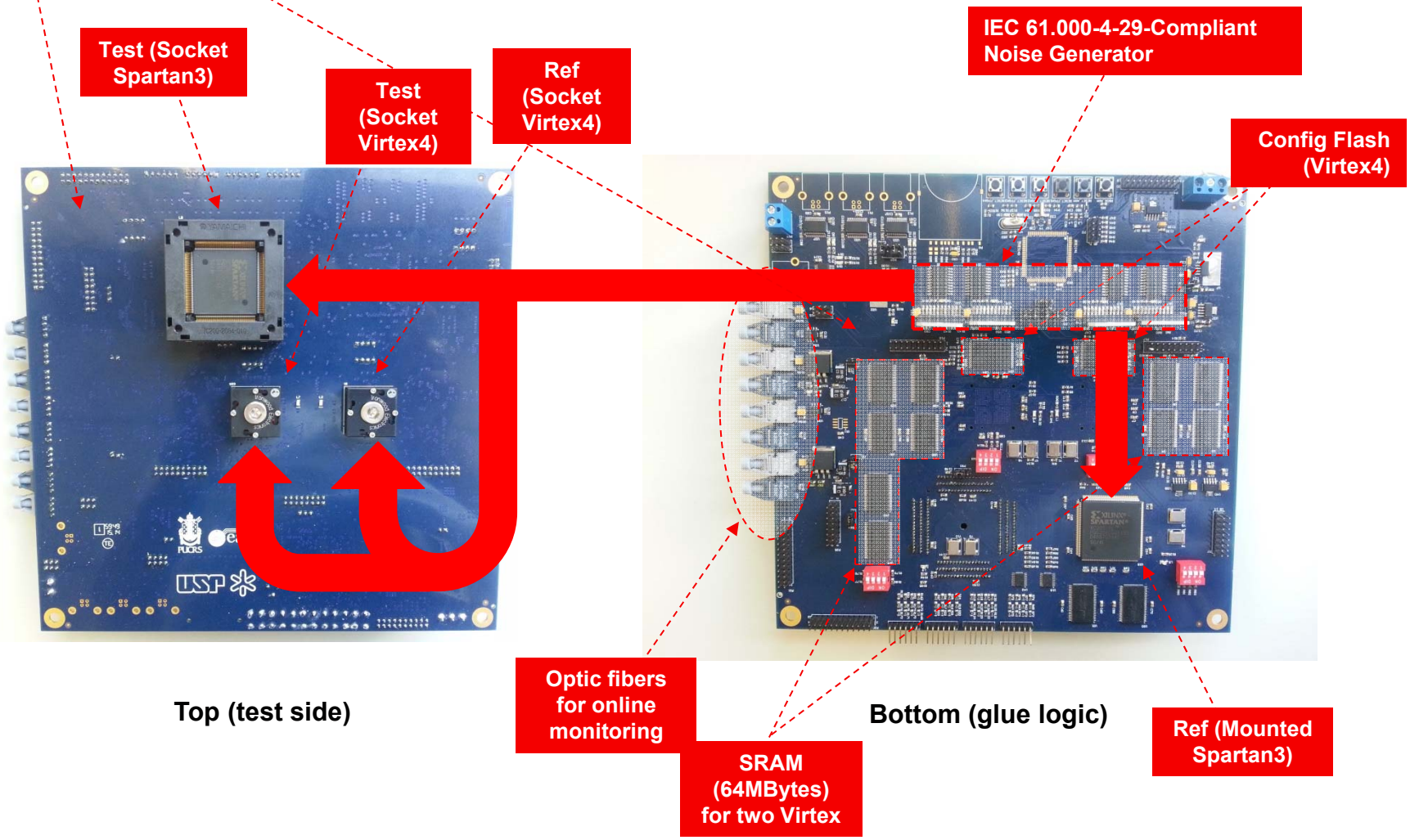
Glue Logic
(backside)

6-layer Daughterboard for Combined EMI x Radiation tests:

(c) Top (test side)

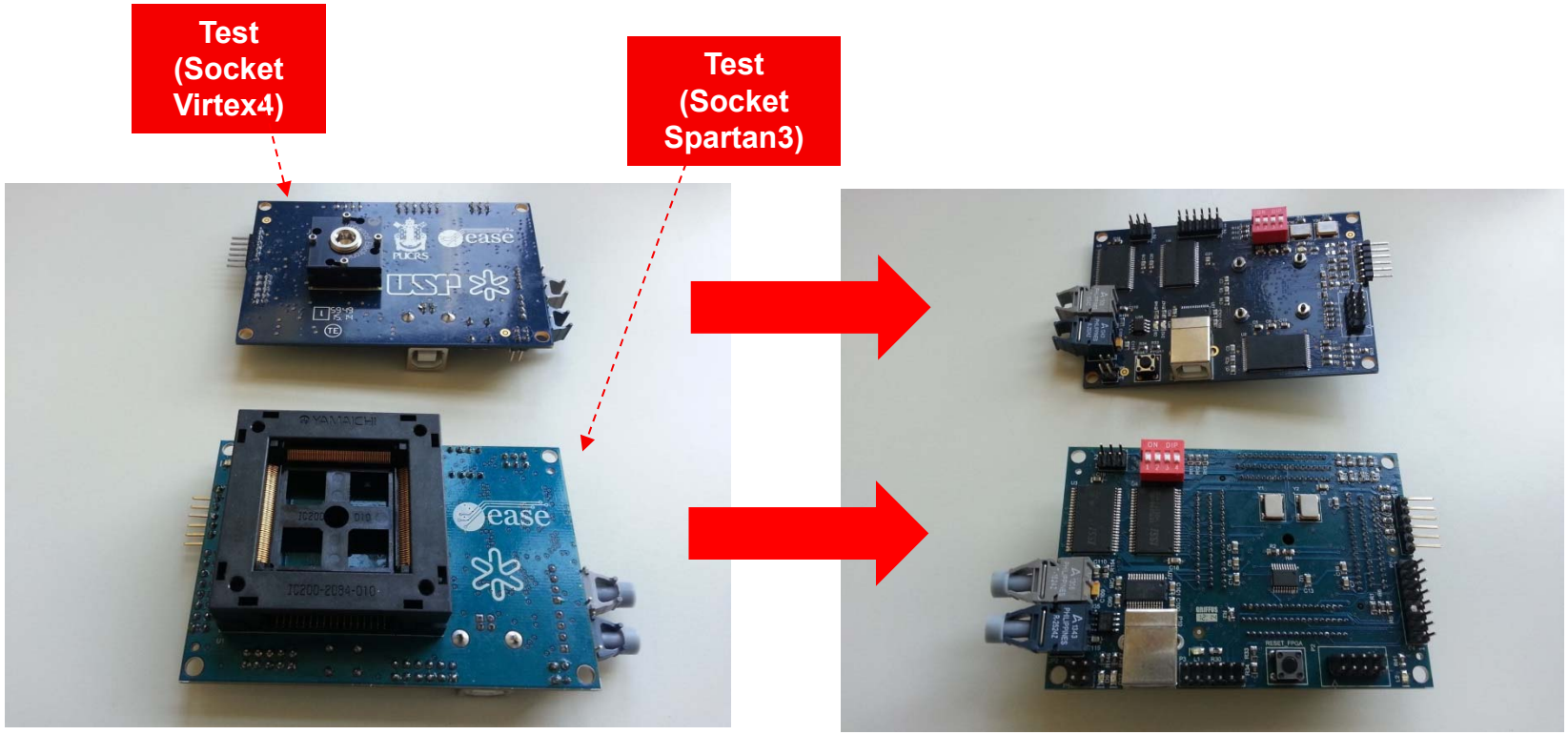
(d) Bottom (glue logic)

Platform (HW parts)



12-layer Motherboard for Combined EMI x Radiation tests

Platform (HW parts)



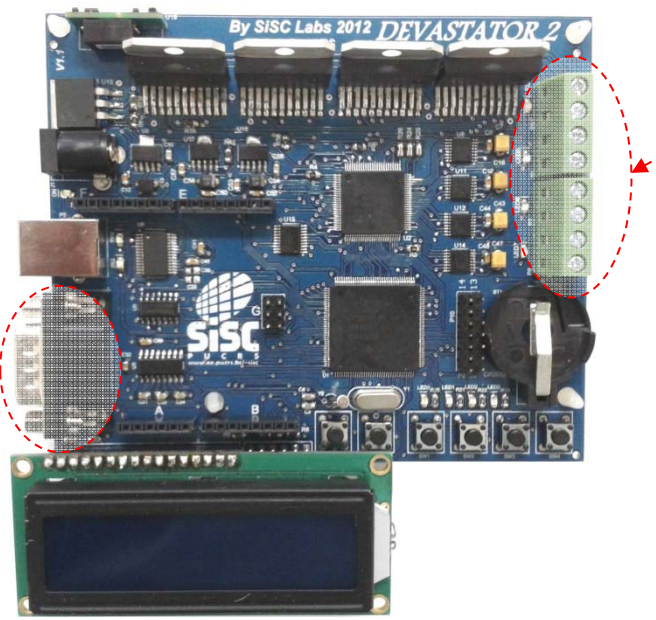
Top (test side)

Bottom (glue logic)

6-layer Daughterboards for Combined EMI x Radiation tests

Platform (HW parts)

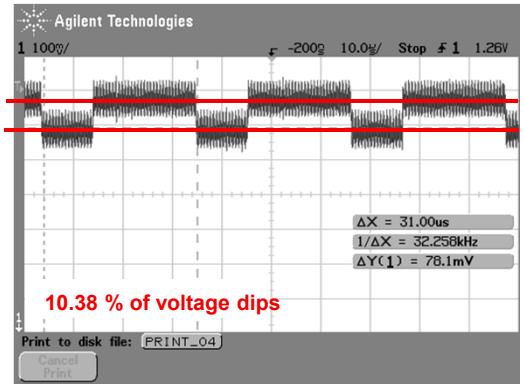
IEC 61.000-4-29-Compliant External EMI Noise Injector



Power-Supply to the CUT

1.2 volts

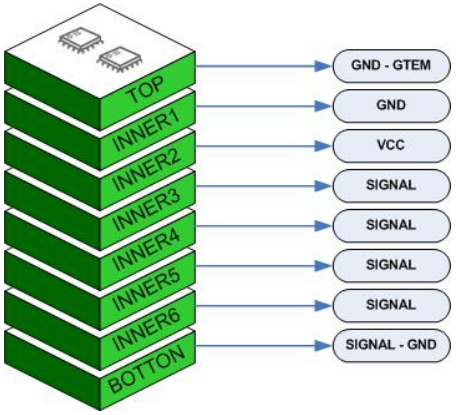
1.07 volts



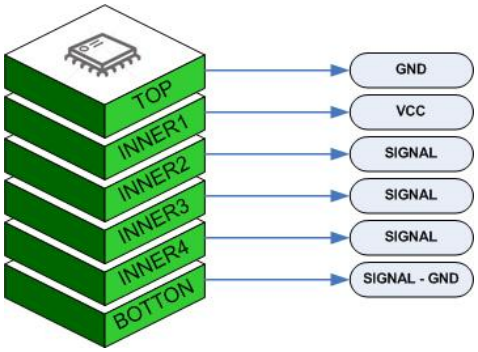
Conducted noise injected in the CUT

Configurable from PC (Serial port)

Platform (HW parts)



(a)



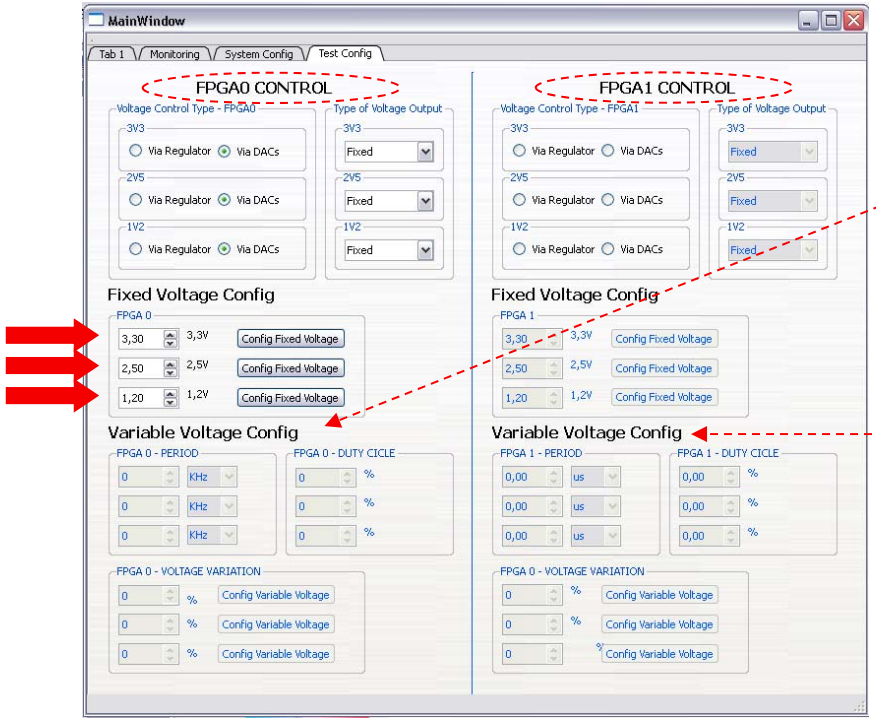
(b)

Layer distribution for:

(a) **EM immunity board (Motherboard), and**

(b) **TID /Burn-in immunity board (Daughterboard)**

Platform (SW parts)



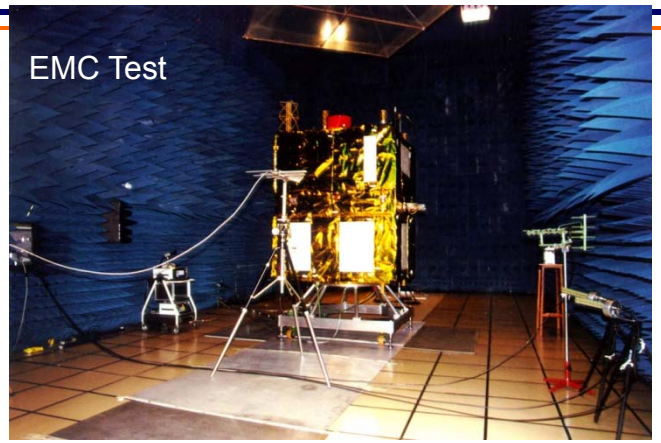
Test Type	Level	Percentage of the nominal DC voltage
Ripple	1	2
	2	5
	3	10
	4	15
	X	X

Test Type	Test Level (%)	Duration (s)
Voltage Dips	40, 70 or X	0.01
		0.03
		0.1
		0.3
		1
		X

Programming interface of the platform: screenshot of the configuration environment to perform tests according to the IEC stds 61.000-4-17 and 61.000-4-29

Brazilian Space Program

- Star Tracker (Navigation System)
- Onboard Telecommunication System



Final system integration

Platform was re-designed to qualify defense-grade and COTS components to replace space-grade ones in satelite apps:

- ACTEL MICROSEMI:

Family: **ProASIC3**, Tech: **Flash**, 250nm

Family: **RTAX**, Tech: **Antifuse**, 250 nm

- AEROFLEX COBHAM:

Family: **Eclipse**, Tech: **Antifuse**, 250 nm

- XILINX: Family: **Virtex5**, Tech: **SRAM**, 65nm

Experiments

Based on the Platform

Combined Tests: Conducted EMI with TID

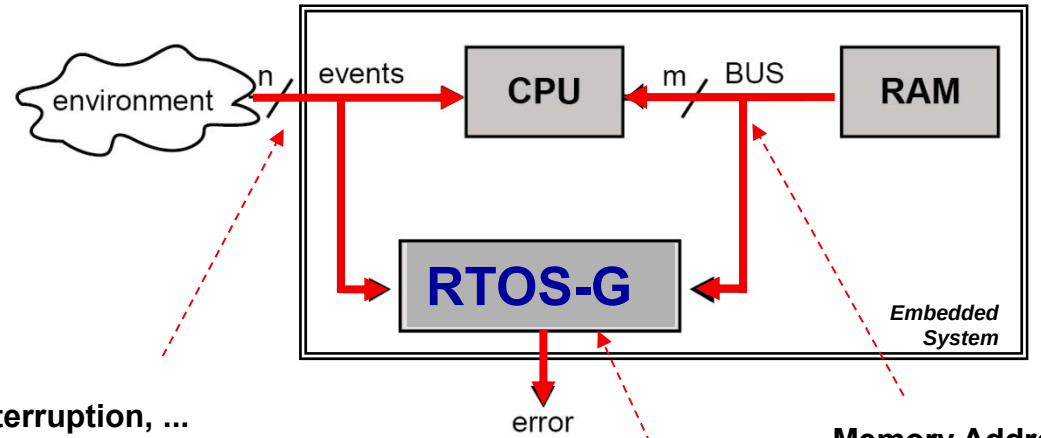
Experiment (1)

IP Core: RTOS-Guardian (RTOS-G), a watchdog to monitor RTOS activity in embedded systems

Some kind of "Passive" Task Scheduler in HW

☞ **the RTOS-G targets faults that ESCAPE detection by the native structures present in the RTOS kernel.**

Experiment (1)



Events: Tick, interruption, ...

(Reference for

Task Context Switching)

Memory Addresses accessed by the processor.

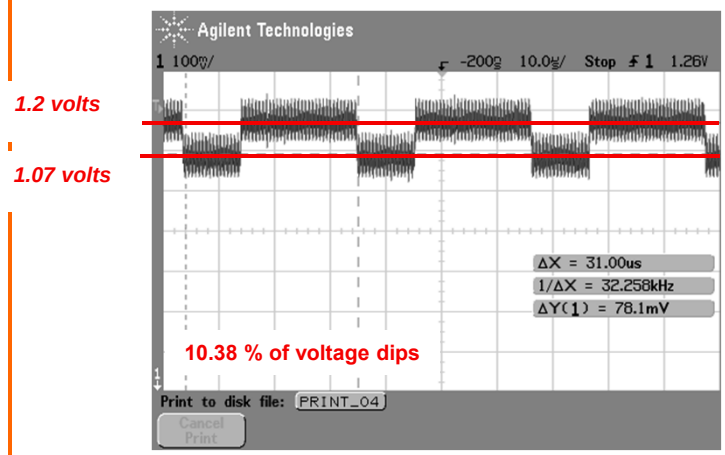
RTOS-G identifies the current task under execution by correlating addresses flowing through the bus with the information stored in an Address Table generated during the compilation process.

Block diagram of the target embedded system

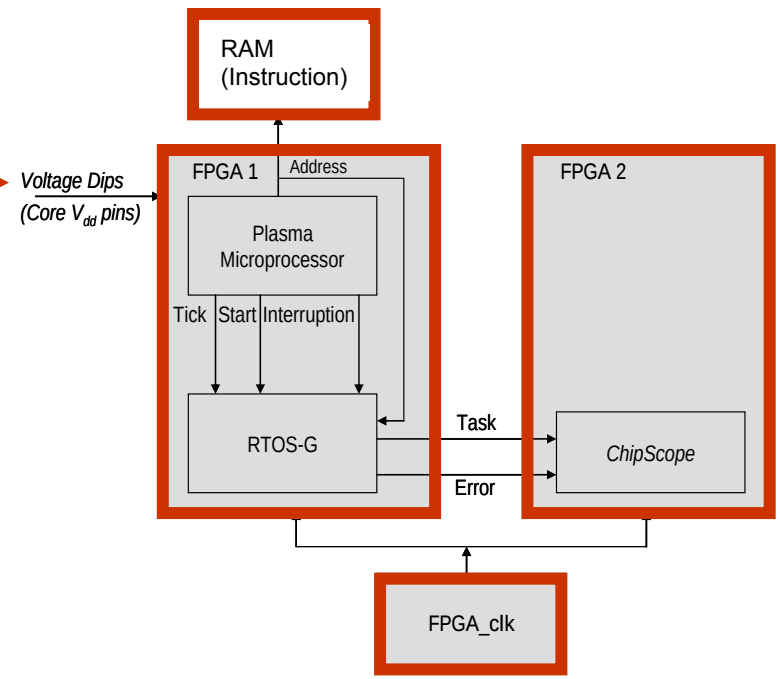
Experiment (1)

Fault injection campaign: *based on the IEC 61.000-4-29 Int. Std. for conducted EMI on the DC input power port of (fresh) FPGA 1*

Voltage dips were randomly injected at the **FPGA 1 V_{dd} input pins** at a frequency of **25.68 kHz**: dips of **~10.83% of the nominal V_{DD}**.



Injected noise at the FPGA power bus (conducted EMI)



Fault injection environment

Experiment (1)

Results for Fault Detection

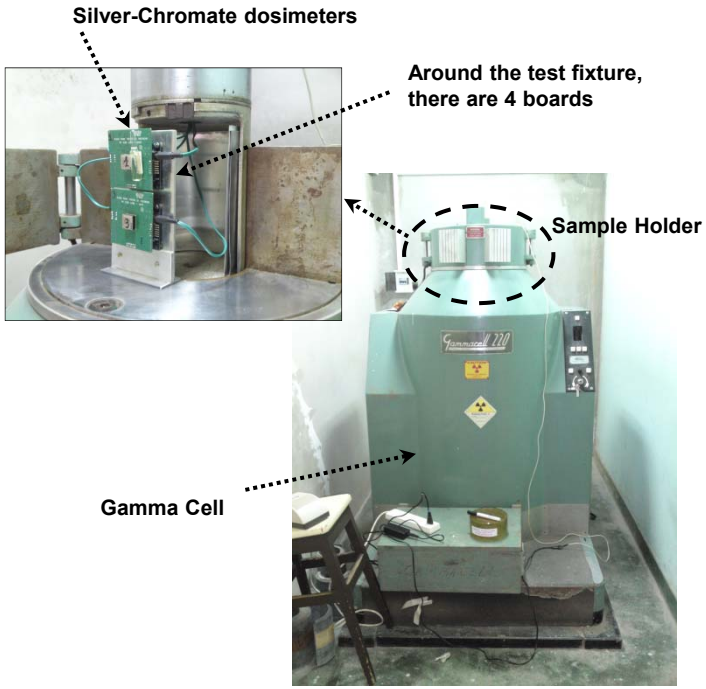
As long as more complex services of the kernel are used, the higher is the RTOS error detection.

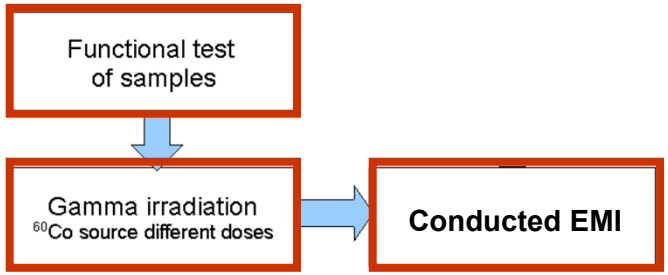
*The native fault detection mechanism (**assert() function**) is called by the kernel every time RTOS runs its services (message queues, semaphores).*

Benchmark	RTOS Kernel [%]	RTOS-G [%]
BM1	2.40	99.90
BM2	25.90	100.00
BM3	45.80	100.00
Average	***24.70***	***99.97***

Experiment (1)

Fault injection campaign: *TID irradiation of FPGA1 in a Gamma Cell with Co^{60}*

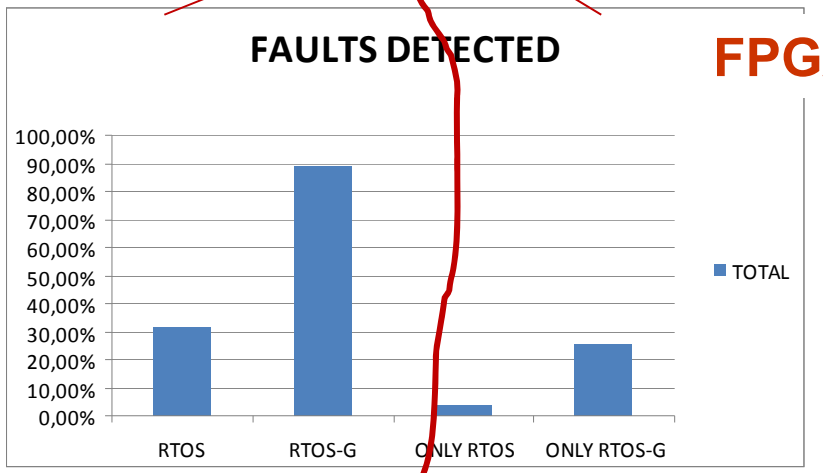




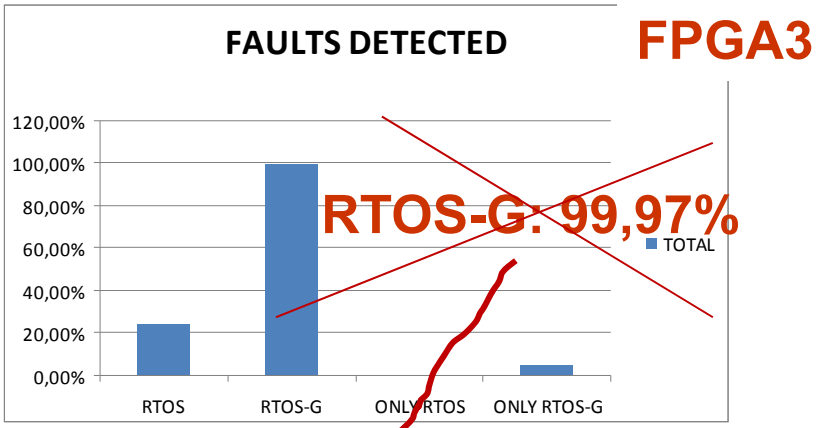
Experiment	FPGA0 (krads)	FPGA1 (krads)	FPGA2 (krads)	FPGA3 (krads)	FPGA4 (krads)
1st experiment, December/2010	0	5.6	51.9	111.0	216.0
2nd experiment, March/2011	0	217.6	263.9	323.0	---

Experiment (1)

~~RTOS: 24,70%~~

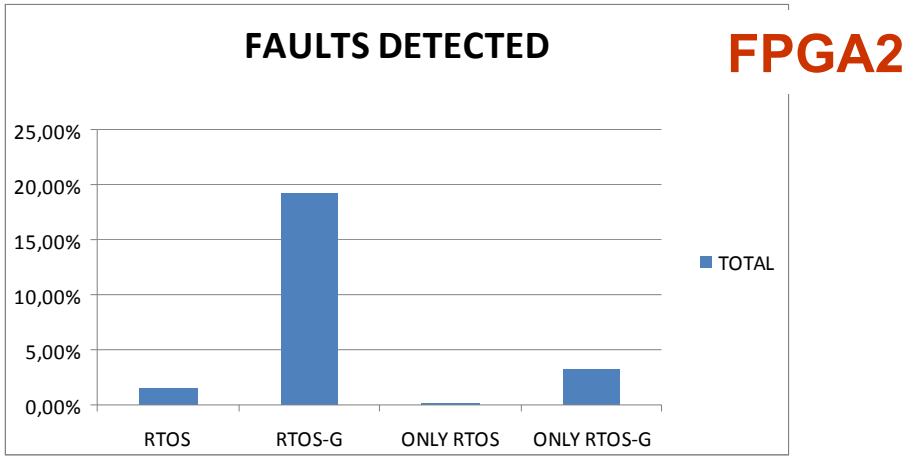


RTOS: 18,00%



~~RTOS-G: 99,97%~~

RTOS-G: 68,67%



Combined Tests: Radiated EMI with TID

Experiment (2)

Combined tests:

TID (Co^{60}) and Radiated-EM Immunity

1st Part*: **4 fresh FPGAs Virtex4** (XC4VFX12-10SF363) were characterized to radiated EM Immunity.

* *based on **IEC 61.132-2 Std** (TEM Cell Method, anechoic chamber).*

Test method conditions:
- EM field range*:* from 10 to 120 v/m (volts/meter);
- Radiated signal frequency range*:* [150kHz - 1GHz];
- Signal modulation: AM Carrier 80% modulation at 1kHz, Horizontal Polarization.

2nd Part**: aging by TID exposition:

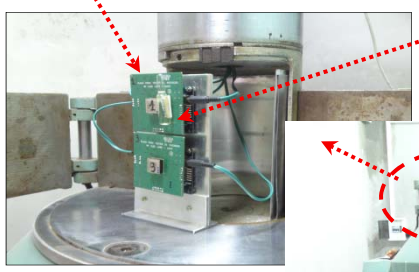
- *Fab.* ***Lot 1****:* 2 FPGAs received a total dose of **160 krads**
- *Fab.* ***Lot 2****:* 2 FPGAs received a total dose of **336 krads**

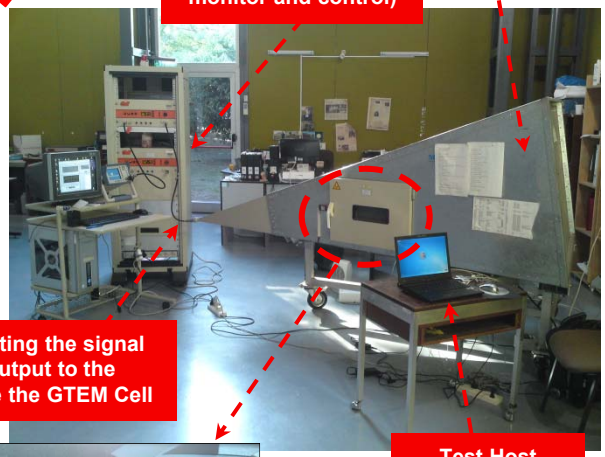
** *based to **MIL-883H Std** (1019.8 Method for TID radiation testing), room temperature, dose rate: 155.5 rads/s.*

Experiment (2)

Combined tests:

TID (Co^{60}) and Radiated-EM Immunity





Radiation source used for gamma radiations.

Environment for radiated EM immunity measurements.

Test Environment

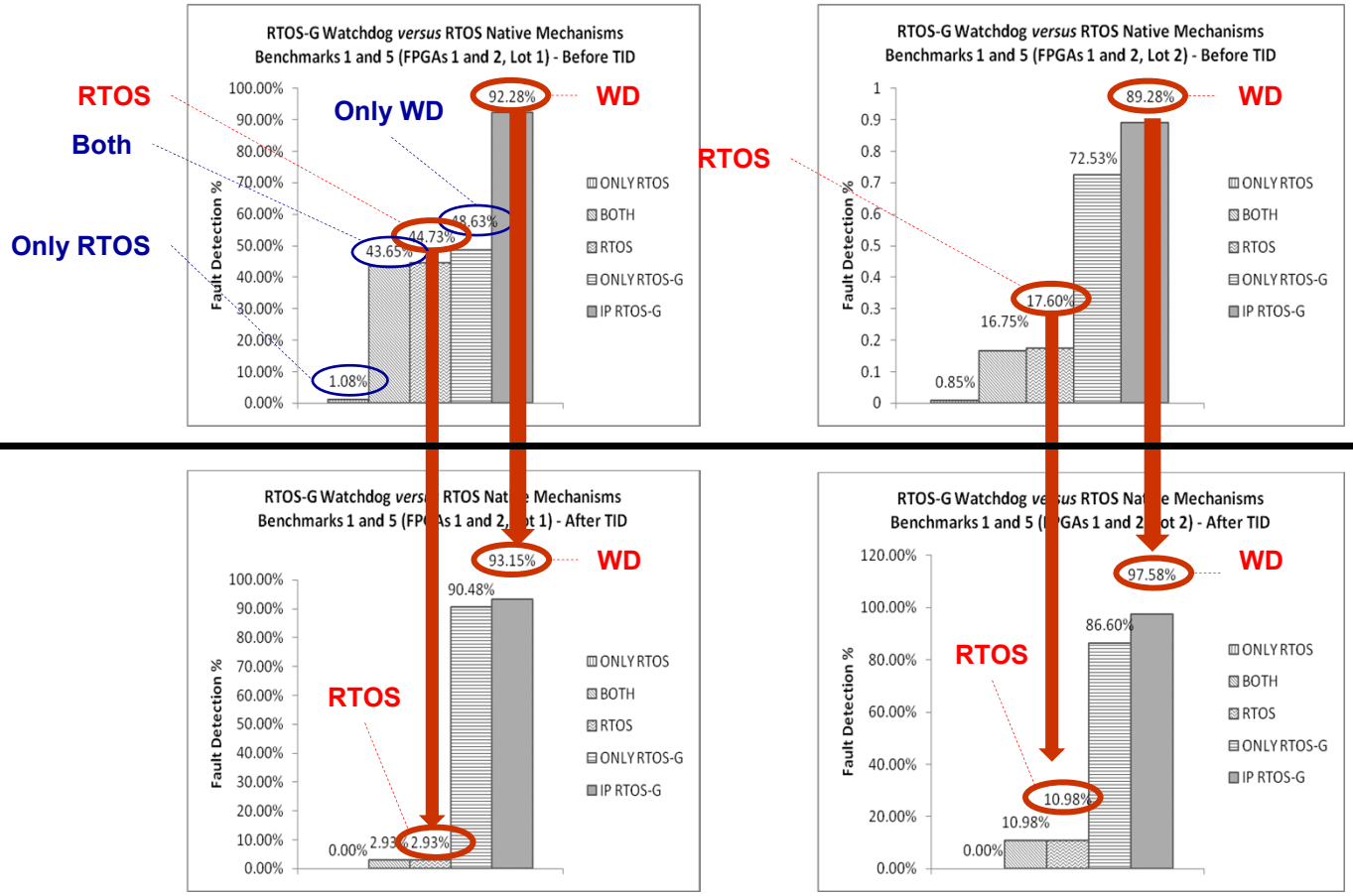
Experiment (2)

Combined tests:

TID (Co^{60}) and Radiated-EM Immunity

irradiated EMI, before TID

irradiated EMI, After TID



Comparison between the fault detection capability of the WD against the RTOS native fault detection mechanisms for fresh and aged FPGAs operating in an EMI-exposed environment

Experiment (2)

Combined tests:

TID (Co^{60}) and Radiated-EM Immunity

Frequencies at which it was observed system failure during EM-immunity test (Fixed EM Field: 80 v/m) for 160krads and 340krads deposited on FPGAs

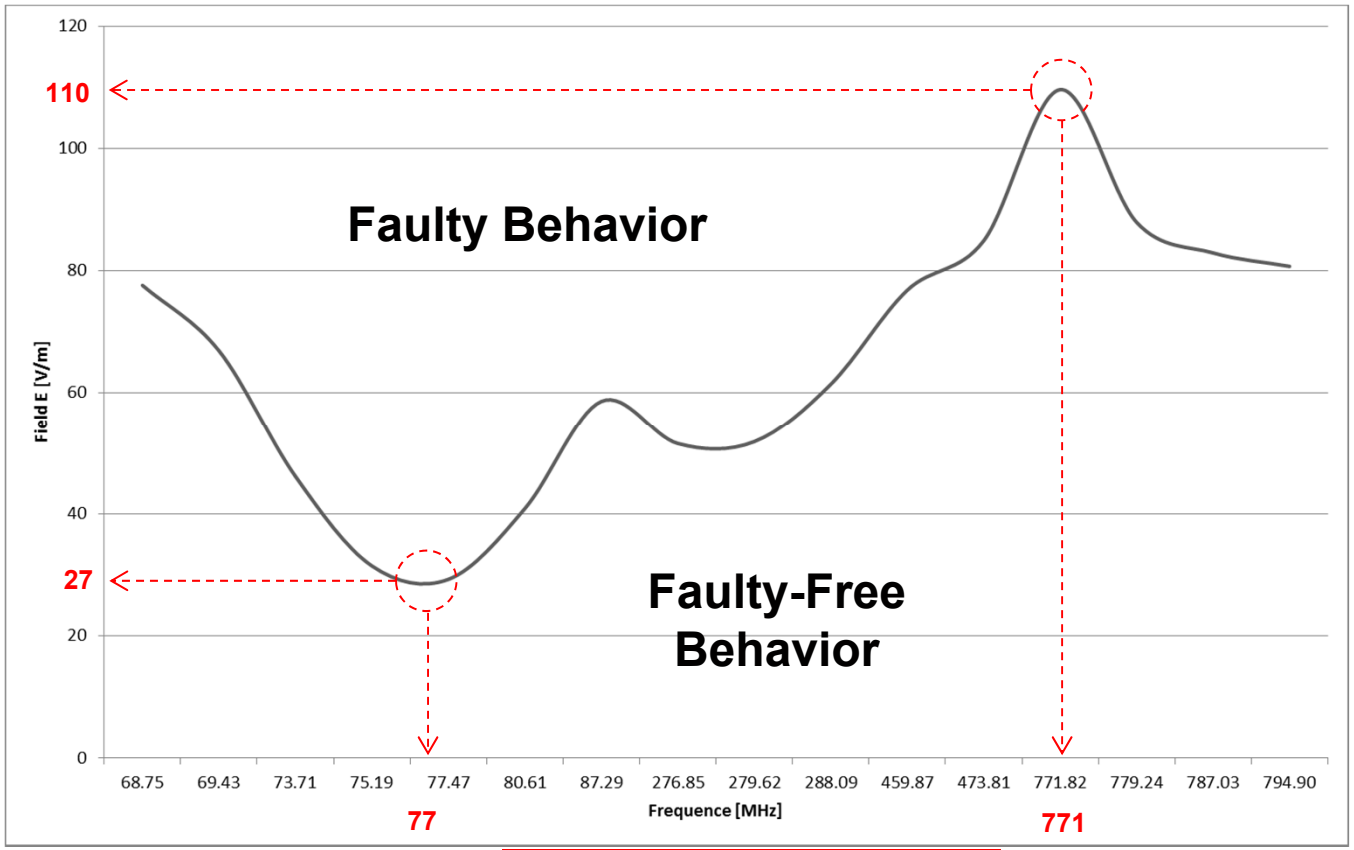
	Frequencies or [frequency ranges] at which the system failed (MHz)	
	1st Experiment (Initial dose: 160 krad)	**2nd Experiment** (Fully aged with 340 krad)
FPGA 1 (Lot 1)	67.39	[68.07 - 93.59]
	68.07	[276.85 - 299.79]
	68.75	[311.86]
	79.81	[459.87 - 473.81]
	99.34	[771.52 - 794.90]
	100.34	
	166.67	
	168.34	
	170.02	
	178.69	
	258.22	
	260.81	
	263.41	
	266.05	
	315.08	
	999.32	

Experiment (2)

Combined tests:

TID with Co^{60} and Radiated-EM Immunity

Electromagnetic immunity for the Xilinx Virtex4 (XC4VFX12-10SF363).
Results for FPGA 1 (*Lot 1*) fully aged with 340 krad of Co^{60}.
Immunity test = IEC 62.132-2 TEM-Cell Test Method, on July 2013.



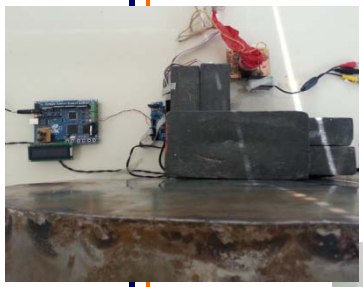
Sensitivity Function

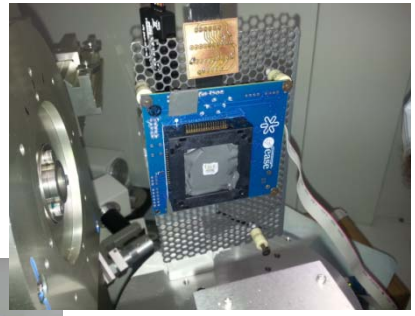
Combined Tests: Conducted EMI with TID and SEU

Experiment

Goal:

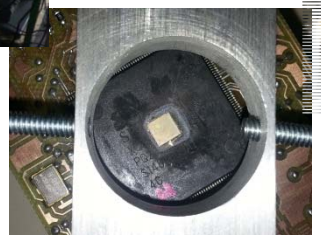
SEU sensitivity w.r.t. imprint effect, V_{DD} disruption and TID in a **Xilinx/Spartan3 FPGA** (CMOS 90nm) (XC3S500E-4PQ208)





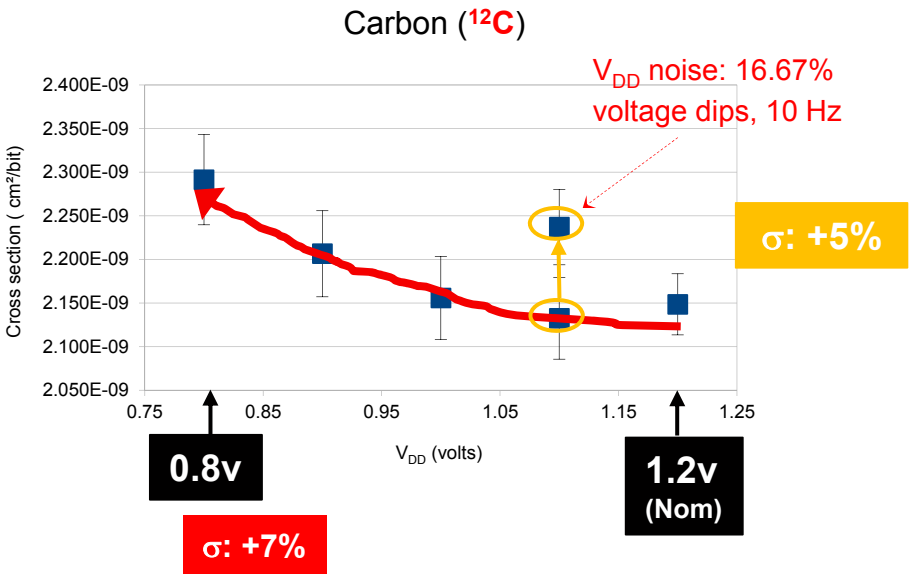
TID
(X-Ray, AmBe)

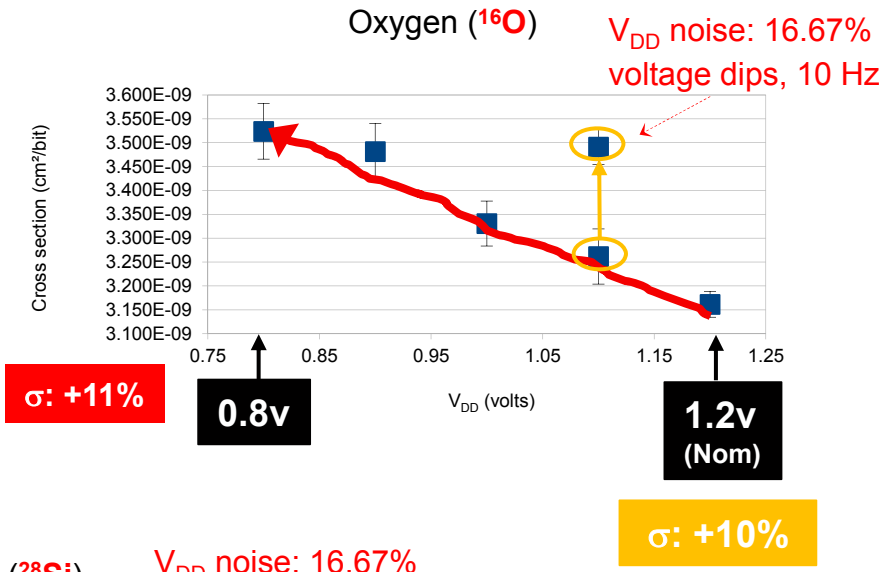
SEU
(Heavy Ions Accelerator)

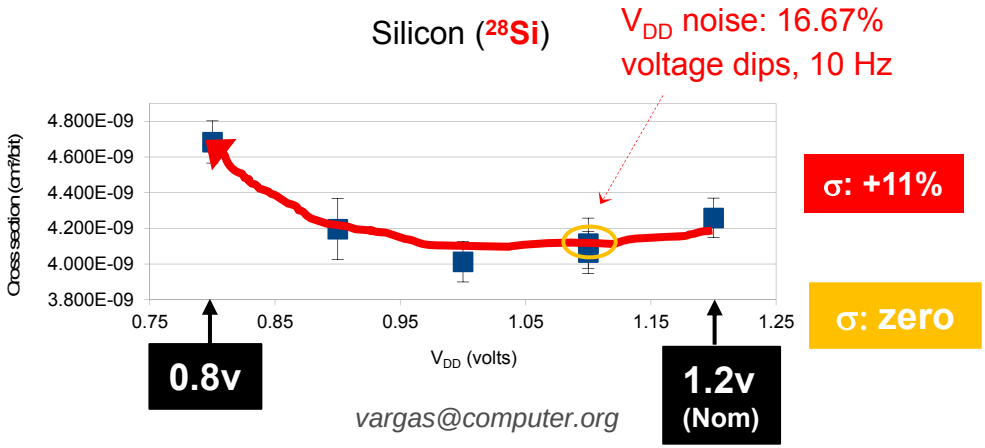


Experiment

(Configuration Bitstream) Cross Section as function of Power Supply (V_{DD}) Disturbance (**Fresh FPGA**)







vargas@computer.org

Experiment

Imprint Effect:

When a memory element remains for a long period storing **the same logical level** (“0” or “1”) while being irradiated for high dose rates, **it tends to maintain this value during the rest of its lifetime (**similar to the **“stuck-at fault” Model** widely used by industry**)**.

We have deposited **750 krad** and **950 krad** on two **Xilinx/Spartan3** FPGAs storing the pattern “all 0’s” in the BRAMs (“hard” pattern) (same fabrication lot)

Experiment

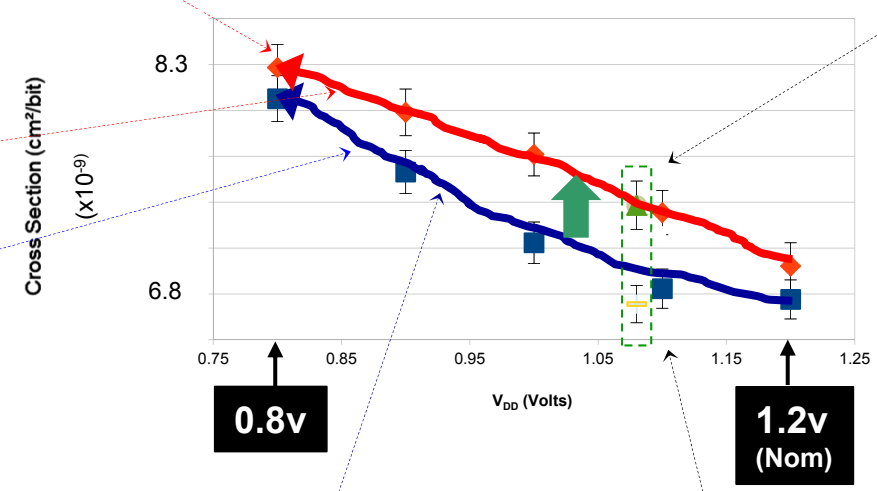
(BRAM) Cross Section as function of Power Supply (V_{DD}) Disturbance
(**Irradiated FPGA with 750 krad**)

750 krad, pattern "all 1's" ("soft")

BRAM Cross Section as function of V_{DD} reduction/noise
Considering "Imprint Effect" [750 krad], ^{16}O (50 MeV)

σ: +27.6%

σ: +29.5%



V_{DD} noise: 16.67%voltage dips, 10 Hz, pattern "all 1's" ("soft").
σ Degradation w.r.t. the nominal V_{DD}: 8.33%

σ degradation induced by imprint effect: +13%

750 krad, pattern "all 0's" ("hard")

V_{DD} noise: 16.67%voltage dips, 10 Hz, pattern "all 0's" ("hard").
σ Degradation w.r.t. the nominal V_{DD}: 0%

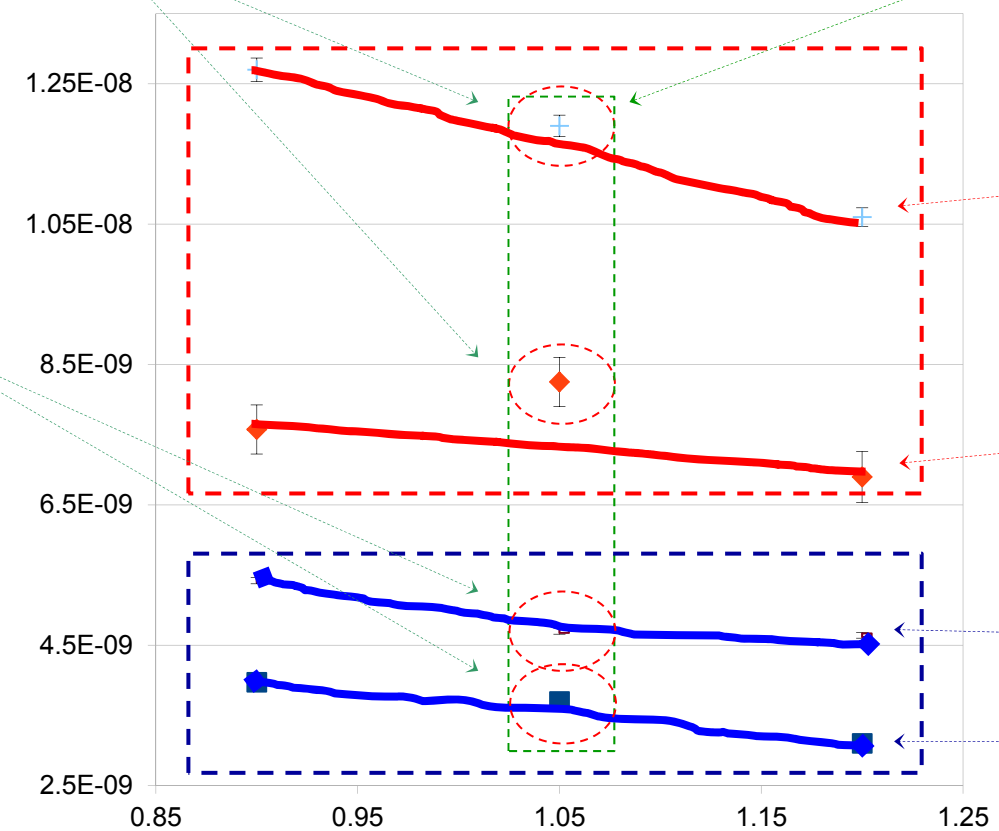
Experiment

(BRAM vs. Config) Cross Section as function of Power Supply (V_{DD}) Disturbance
(**Irradiated FPGA with 950 krad, ^{28}Si**)

σ Degradation w.r.t. the nominal V_{DD}: 16%

V_{DD} noise: 25%voltage dips, 5kHz

σ Degradation w.r.t. the nominal V_{DD}: 10.4%



BRAM, 950 krad Pattern "All "1's" ("soft")

BRAM, Fresh Pattern "All "1's" ("soft")

Config, 950 krad

Config, Fresh

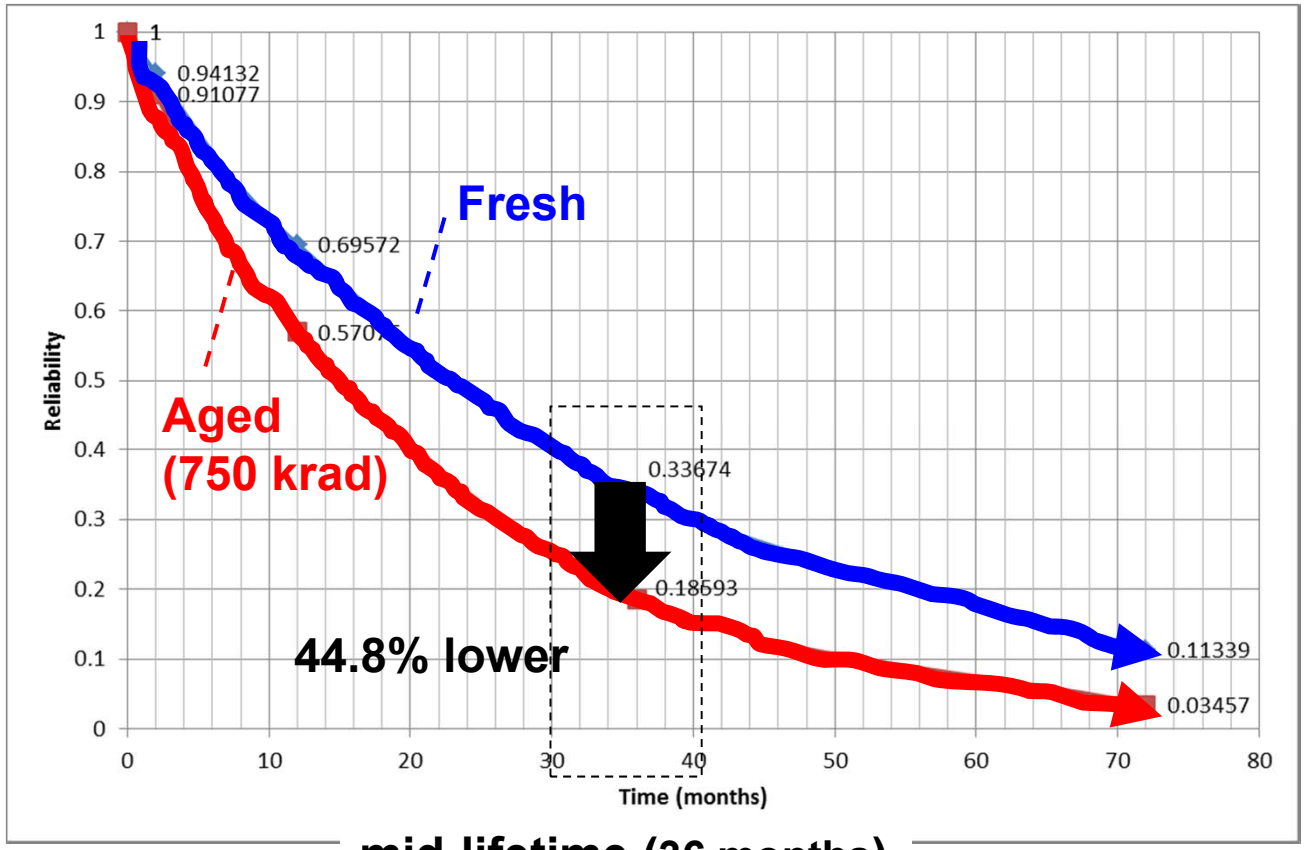
BRAM ~ x4.3 more sensitive to SEU than Config mainly due to the imprint effect

SiSC PUCRS

Experiment

BRAM Reliability per Bit

Power Supply (V_{DD}): 0.85 volts
SEU Results for Fast Neutrons (^{241}AmBe), [2 – 11] MeV
(**Fresh x Irradiated FPGA with 750 krad, ^{28}Si**)



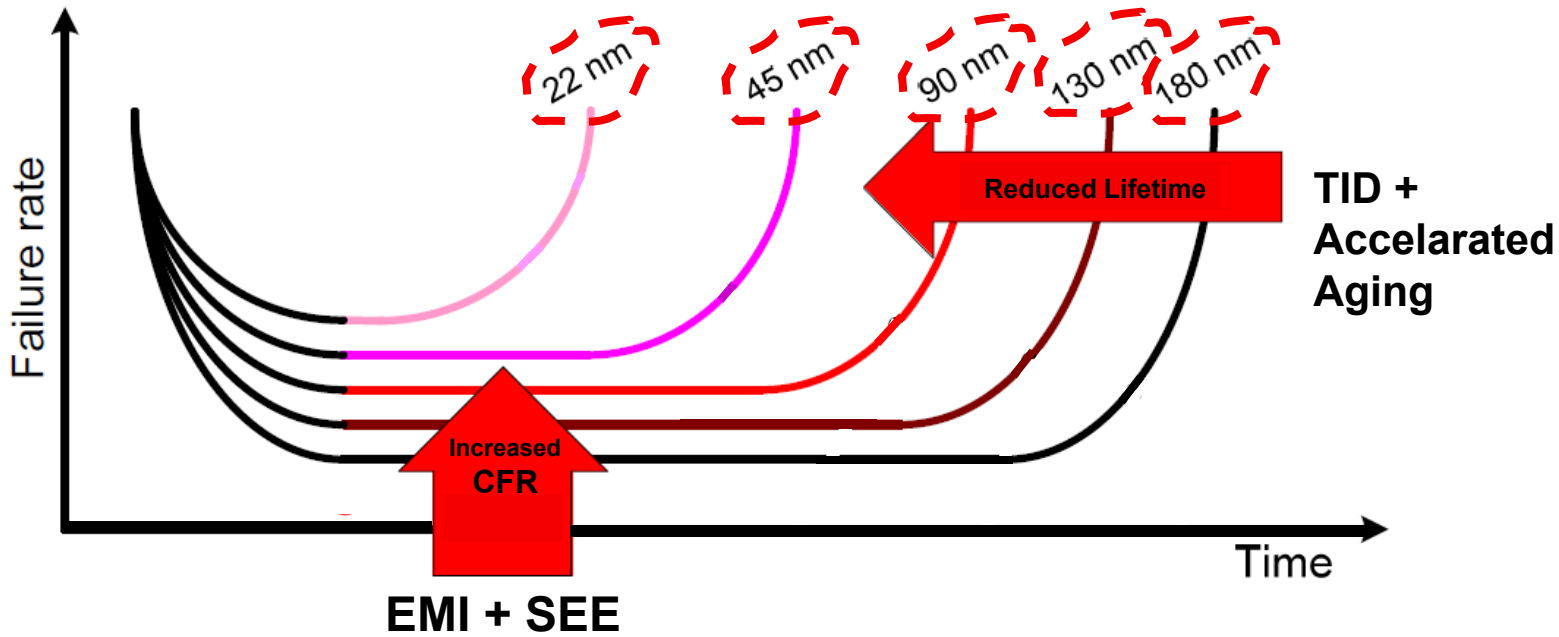
mid-lifetime (36 months)

Mainly induced by the "soft" pattern

Conclusions

Bath Tube for nano-IC's is shrinking:

Combined System Failure Rate ↑ & Lifetime ↓



Ref: DATE 2010, Lin Huang et. al.

Events addressing the presented topics …

LATS2016

17th IEEE Latin-American Test Symposium
Foz do Iguaçu, Brazil, 6th - 8th April 2016
TTEP Day 9th April 2016

General Chairs:
Leticia Bolzani Poehls – PUCRS, Brazil
leticia@poehls.com

Yervant Zorian – SYNOPSYS, USA
yervant.zorian@synopsys.com

Past General Chair:
Victor Champac – INAOE, Mexico

Honorary Chair:
Fabian Vargas – PUCRS, Brazil

Local Chair:
Andre Mariano - UFPR, Brazil

Program Chairs:
Matteo Sonza Reorda – Politecnico di Torino, Italy
Tiago Balen – UFRGS, Brazil

Special Session Chair:
Vishwani Agrawal – Auburn University, USA

Panel Chairs:
Raoul Velazco – TIMA Laboratories, France
Fernanda Kastensmidt – UFRGS, Brazil

CALL FOR PAPERS

The IEEE Latin-American Test Symposium (LATS, previously Latin-American Test Workshop - LATW) is a recongnized forum for test and fault tolerance professionals and technologists from all over the world, in particular from Latin America, to present and discuss various aspects of system, board, and component testing and fault-tolerance with design, manufacturing and field considerations in mind. Presented papers are also published in the IEEE Xplore Digital Library. The best papers of the 17th LATS will be invited to re-submit to IEEE Design and Test of Computers, IEEE Transactions on Computer-Aided Design, Journal of Electronic Testing: Theory and Applications - JETTA (Springer) and Journal of Low Power Electronics - JOLPE (American Scientific Publishers).

Topics of interest include but are not limited to:

- Analog Mixed Signal Test
- Automatic Test Generation
- Built-In Self-Test
- Defect-Based Test
- Design and Synthesis for Testability
- Design for Electromagnetic Compatibility
- Design for Reliable Embedded Software
- Design Verification/Validation
- Economics of Test
- Fault Analysis and Diagnosis
- Fault Modeling and Simulation
- Fault-Tolerance in HW/SW
- Fault-Tolerant Architectures
- Memory Test and Repair
- On-Line Testing
- Process Control and Measurements
- Radiation/EMI
- Hardening Techniques
- Software Fault-Tolerance
- Software On-Line Testing
- System-on-Chip Test
- Test Resource Partitioning
- Yield Optimization
- Hardware Security

APEMC
2016
Shenzhen

www.apemc.org May 18-21, 2016 Shenzhen, China

Call for Pap

2016 APEMC Topical Mini-Symposium on IC EMC

The topical mini-Symposium on IC-EMC is organized as a special track under the 2016 APEMC, which will be held in Shenzhen, China, May 18 to 21, 2016. Prospective authors are invited to submit original papers on their latest research results. Presented papers are also published in the ***IEEE Xplore* Digital Library**. Topics of interest include, but are not limited to:

Symposium Topics

- Design of 2D and 3D system-on-chip (SoC) for EMC
- Hardware-software co-design and integration for IC EMC
- Emission and immunity-aware IC design
- ESD immunity techniques at IC level
- Signal and power integrities at IC level
- Combined effects of radiation and aging on IC EM sensitivity
- Harsh environment effects on IC EM sensitivity
- IC EMC for avionics and automotive applications
- EMC-aware analog and mixed signal circuits
- RF ICs EMC
- IC-level measurement techniques for EMC
- IC-level modeling techniques for EMC
- EMC simulation of integrated circuits
- EMC in Microwave Integrated Circuits
- EMC-aware software solutions
- FPGA-based embedded systems and EMC

General Chair:

Er-Ping Li
erpingli@ieee.org

Topical Symposium Chairs:

Sonia Ben Dhia
INSA Euro-Méditerranée, UEMF, Morocco
LAAS CNRS, Toulouse, France
sonia.bendhia@insa.ueuromed.org

Bernd Deutschmann
Graz University of Technology, Austria
bernd.deutschmann@tugraz.at

Fabian Vargas
Catholic University - PUCRS, Brazil
vargas@computer.org

Shih-Yi Yuan
Feng Chia University, Taiwan
syyuan@fcu.edu.tw

Scientific Committee:

A. Boyer, LAAS CNRS, France A. Barić, FER, Croatia
P. Besse, Freescale, France
M. Coenen, EMCMCC bv, Netherlands
C. Marot, AIRBUS Group, France
F. Fiori, Polito Torino, Italy
A. Durier, IRT Toulouse, France
M. Ramdani, ESEO, France

Thank you for your attention …